NOVOSENSE
纳芯微电子

NSI6622

High Reliability Isolated Dual-Channel Gate Driver

Datasheet (EN) 1.3

Product Overview

NSI6622 is a family of high reliability isolated dual-channel gate driver ICs which can be designed to drive power transistor up to 2MHz switching frequency. Each output could source 4A and sink 6A peak current with fast 25ns propagation delay and 5ns maximum delay matching.

The NSI6622 provides 2500Vrms isolation per UL1577 in 5*5mm LGA13 package, 3000Vrms isolation in SOP16 package, and 5700Vrms isolation in SOW16 or SOW14 package. System robustness is supported by 150kV/μs typical common-mode transient immunity (CMTI).

The driver operates with a maximum supply voltage of 25V, while the input-side accepts from 2.7V to 5.5V supply voltage. Under voltage lock-out (UVLO) protection is supported by all the power supply voltage pins.

Key Features

- Isolated dual channel driver
- Input side supply voltage: 2.7V to 5.5V
- Driver side supply voltage: up to 25V with UVLO
- 4A peak source and 6A peak sink output
- High CMTI: ±150kV/μs
- 19ns typical propagation delay
- 5ns maximum delay matching
- 6ns maximum pulse width distortion
- Accepts minimum input pulse width 20ns
- Operation temperature: -40℃~125℃
- RoHS & REACH Qualified

Applications

- Isolated DC-DC and AC-to-DC power supplies
- DC-to-AC solar inverters
- Motor drives and EV charging
- UPS and battery chargers

Safety Regulatory Approvals

- UL recognition:
  - SOW16/SOW14: 5700V_{rms} for 1 minute per UL1577
  - SOP16: 3000V_{rms} for 1 minute per UL1577
  - LGA13: 2500V_{rms} for 1 minute per UL1577
- DIN VDE V 0884-11:2017-01
- CSA component notice 5A
- CQC certification per GB4943.1-2011

Device Information

Part Number	Package	Body Size
NSI6622A-DSWR	SOW16	10.3×7.5×2.65mm
NSI6622B-DSWR	SOW16	10.3×7.5×2.65mm
NSI6622C-DSWR	SOW16	10.3×7.5×2.65mm
NSI6622A-DSWKR	SOW14	10.3×7.5×2.65mm
NSI6622B-DSWKR	SOW14	10.3×7.5×2.65mm
NSI6622C-DSWKR	SOW14	10.3×7.5×2.65mm
NSI6622A-DSPNR	SOP16	9.9×3.9×1.75mm
NSI6622B-DSPNR	SOP16	9.9×3.9×1.75mm
NSI6622C-DSPNR	SOP16	9.9×3.9×1.75mm
NSI6622A-DLAR	LGA13	5×5×0.91mm
NSI6622B-DLAR	LGA13	5×5×0.91mm
NSI6622C-DLAR	LGA13	5×5×0.91mm

Functional Block Diagram

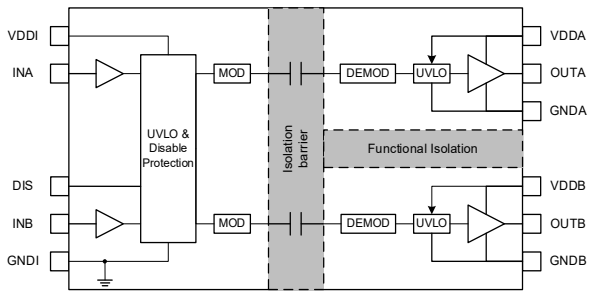


Figure 0.1 NSI6622 Block Diagram

INDEX

1. Pin Configuration and Functions

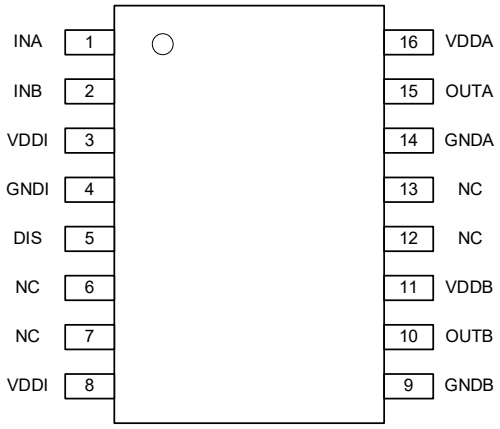


Figure 1.1 NSI6622 SOW16/SOP16 Package

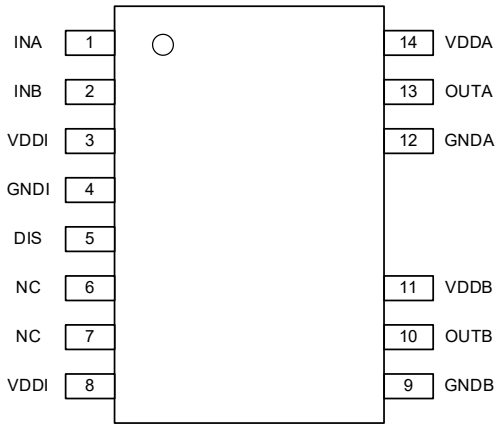


Figure 1.2 NSI6622 SOW14 Package

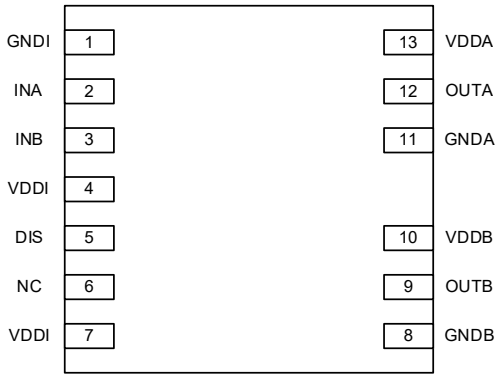


Figure 1.3 NSI6622 LGA13 Package

Table 1.1 NSI6622 Pin Configuration and Description

PIN NO.			SYMBOL	FUNCTION
LGA13	SOP16	SOP14		
1	4	4	GND	Input-side ground reference.
2	1	1	INA	TTL/CMOS compatible input signal for channel A with internal pull down to GND. It is recommended to connect this pin to GND if not used.
3	2	2	INB	TTL/CMOS compatible input signal for channel B with internal pull down to GND. It is recommended to connect this pin to GND if not used.
4, 7	3, 8	3, 8	VDDI	Input-side supply voltage. It is recommended to place a bypass capacitor from this pin to GND as close as possible.
5	5	5	DISABLE	Disables the isolator inputs and driver outputs if asserted high, enables if asserted low or left open. It is recommended to connect this pin to GND if not used.
8	9	9	GNDB	Ground for output channel B
9	10	10	OUTB	Output gate driver for channel B
10	11	11	VDDB	Supply voltage for channel B
11	14	12	GNDA	Ground for output channel A
12	15	13	OUTA	Output gate driver for channel A
13	16	14	VDDA	Supply voltage for channel A
6	6,7,12[1)],13	6,7	NC	Not connected

1) For SOP16 package, Pin 12 has been connected to GNDB. Suggest not to connect Pin12 with other nets.

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit
Input Side Supply Voltage	VDDI to GNDI	-0.3	6	V
Output Side Supply Voltage	VDDA to GNDA, VDDB to GNDB	-0.3	30	V
Input Signal Voltage	INA, INB, DIS to GNDI	-0.3	V_{VDDI}+0.3	V
	INA, INB, DIS to GNDI, Transient for 50ns	-5	V_{VDDI}+0.3	V
Output Signal Voltage	OUTA to GNDA, OUTB to GNDB	-0.3	V_{VDDA}+0.3 V_{VDDB}+0.3	V
	OUTA to GNDA, OUTB to GNDB, Transient for 200ns	-2	V_{VDDA}+0.3 V_{VDDB}+0.3	V
Channel A to Channel B Voltage	GNDA to GNDB in LGA13 package		700	V
	GNDA to GNDB in SOP16&SOW16 package		1500	V
	GNDA to GNDB in SOW14 package		1850	V
Junction Temperature	T_J	-40	150	°C
Storage Temperature	T_{stg}	-65	150	°C

3. ESD RATINGS

	Ratings	Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD ● All pins	±4000	V
	Charged device model (CDM), per AEC-Q100-011-RevB ● All pins	±1500	V

4. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit
Input Side Supply Voltage	VDDI to GNDI	3	5.5	V
Driver Side Supply Voltage	VDDA to GNDA, VDDB to GNDB (NSI6622A)	7	25	V
	VDDA to GNDA, VDDB to GNDB (NSI6622B)	9.4	25	V
	VDDA to GNDA, VDDB to GNDB (NSI6622C)	14.2	25	V
Input Signal Voltage	INA, INB, DIS	0	V_{VDDI}	V
Ambient Temperature	T_a	-40	125	°C

5. Thermal Information

Parameters	Symbol	LGA13	SOW16/SOW14	SOP16	Unit
Junction-to-ambient thermal resistance[1]	R_{JA}	209.5	97.0	150.5	°C/W
Junction-to-case(top) thermal resistance[2]	$R_{JC(top)}$	48.4	23.3	21.2	°C/W
Junction-to-top characterization parameter[3]	Ψ_{JT}	41.8	35.8	52.3	°C/W
Junction-to-board characterization parameter[3]	Ψ_{JB}	31.9	39.0	55.6	°C/W

1) Standard JESD51-3 Low Effective Thermal Conductivity Test Board (1s) in an environment described in JESD51-2a.

2) Standard JESD51-3 Low Effective Thermal Conductivity Test Board (1s) by transient dual interface test method described in JESD51-14.

3) Obtained by Simulating in an environment described in JESD51-2a.

6. Specifications

6.1. Electrical Characteristics

VDDI=3.3V or 5V, VDDA=VDDB=12V for NSI6622A/B, VDDA=VDDB=15V for NSI6622C, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at Ta=25℃

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Input Side Supply						
VDDI Quiescent Current	I_{VDDIQ}		0.75	2	mA	INA=0, INB=0
VDDI Operation Current	I_{VDDI}		1.8		mA	Input frequency 500kHz, $C_{OUTA/B}$=15pF
VDDI UVLO Rising Threshold	V_{VDDI_ON}	2.35	2.55	2.75	V	
VDDI UVLO Falling Threshold	V_{VDDI_OFF}	2.15	2.35	2.55	V	
VDDI UVLO Hysteresis	V_{VDDI_HYS}		0.2		V	
Output Side Supply						
Output Side Supply Voltage	V_{VDDA}, V_{VDDB}			25	V	Minimum defined by UVLO
VDDA/B Quiescent Current, per Channel	I_{VDDAQ}, I_{VDDBQ}		1.6	2.5	mA	INA=0, INB=0, VDDx=12V for 6V,8V UVLO; VDDx=15V for 13V UVLO
VDDA/B Operation Current, per Channel	I_{VDDA}, I_{VDDB}		3.2		mA	100pF, 500kHz, VDDx=12V for 6V,8V UVLO; VDDx=15V for 13V UVLO
VDDA/B UVLO Rising Threshold	V_{VDDA_ON}, V_{VDDB_ON}	5.7	6.15	6.5	V	NSI6622A (6V)
VDDA/B UVLO Falling Threshold	V_{VDDA_OFF}, V_{VDDB_OFF}	5.4	5.85	6.2	V	

Parameter	Symbol	Min	Typ	Max	Unit	Comments
VDDA/B UVLO Hysteresis	V_{VDDA_HYS}, V_{VDDB_HYS}		0.3		V	
VDDA/B UVLO Rising Threshold	V_{VDDA_ON}, V_{VDDB_ON}	8.1	8.5	8.9	V	NSI6622B (8V)
VDDA/B UVLO Falling Threshold	V_{VDDA_OFF}, V_{VDDB_OFF}	7.6	8.0	8.4	V	
VDDA/B UVLO Hysteresis	V_{VDDA_HYS}, V_{VDDB_HYS}		0.5		V	
VDDA/B UVLO Rising Threshold	V_{VDDA_ON}, V_{VDDB_ON}	12.7	13.2	13.7	V	NSI6622C (13V)
VDDA/B UVLO Falling Threshold	V_{VDDA_OFF}, V_{VDDB_OFF}	11.7	12.2	12.7	V	
VDDA/B UVLO Hysteresis	V_{VDDA_HYS}, V_{VDDB_HYS}		1		V	
Input Side Characteristic						
Input Pin Pull Down Resistance, INA, INB,	R_{INA_PD}, R_{INB_PD}		100		kΩ	
Input Pin Pull Down Resistance, DIS (EN)	R_{DIS_PD}		100		kΩ	
Logic High Input Threshold	V_{INA_H}, V_{INB_H}, V_{DIS_H}		1.7	2	V	
Logic Low Input Threshold	V_{INA_L}, V_{INB_L}, V_{DIS_L}	0.8	1.1		V	
Input Hysteresis	V_{INA_HYS}, V_{INB_HYS}, V_{DIS_HYS}		0.6		V	
Output Side Characteristic						
Logic High Output Voltage	V_{VDDA}-V_{OUTA_H}, V_{VDDB}-V_{OUTB_H}		0.34		V	I_{out} = 100mA
Logic Low Output Voltage	V_{OUTA_L}, V_{OUTB_L}		55		mV	I_{out} = -100mA
Output Sink Resistance	R_{OUTA_L}, R_{OUTB_L}		0.55		Ω	I_{out} = 100mA
Output Source Resistance	R_{OUTA_H}, R_{OUTB_H}		3.4		Ω	I_{out} = -100mA
Peak Output Sink Current	I_{OUTA-}, I_{OUTB-}		6		A	
Peak Output Source Current	I_{OUTA+}, I_{OUTB+}		4		A	

6.2. Switching Characteristics

VDDI=3.3V or 5V, VDDA=VDDB=12V for NSI6622A/B, VDDA=VDDB=15V for NSI6622C, Ta=-40℃ to 125℃.

Parameter	Symbol	Min	Typ	Max	Unit	Comments
Minimum Pulse Width	t_{PWmin}		10	15	ns	
Propagation Delay	t_{PDHL}, t_{PDLH}	10	25	35	ns	
Pulse Width Distortion $\lvert t_{PDLH}-t_{PDHL}\rvert$	t_{PWD}			6	ns	
Channel to Channel Delay Matching	t_{DMLH}, t_{DMHL}			5	ns	
Output Rise Time (20% to 80%)	t_R		7	16	ns	$C_{OUTA/B}$=1.8nF, verified by design

Output Fall Time (90% to 10%)	t_F		6	12	ns	$C_{OUTA/B}$=1.8nF, verified by design
Shutdown Time from Disable True	t_{DIS}			40	ns	
Recovery Time from Disable False	t_{EN}			40	ns	
VDDI Power-up Time Delay (Time from VDDI = VDDI_ON to OUTA/B = INA/B)	t_{start_VDDI}		8.5	15	µs	INA or INB tied to VDDI
VDDA/B Power-up Time Delay (Time from VDDA/B = 2V to OUTA/B = INA/B)	t_{start_VDDA}, t_{start_VDDB}		18	30	µs	INA or INB tied to VDDI; $C_{OUTA/B}$=1.8nF
Common Mode Transient Immunity	CMTI	100	150		kV/µs	verified by design

6.3. Typical Performance Characteristics

VDDI = 3.3 V, VDDA = VDDB = 12 V, TA = 25°C. Output has no load unless otherwise noted.

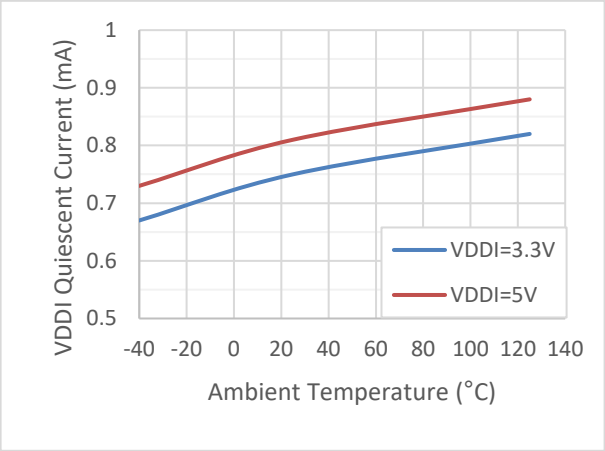


Figure 6.1 VDDI Quiescent Current vs Temperature

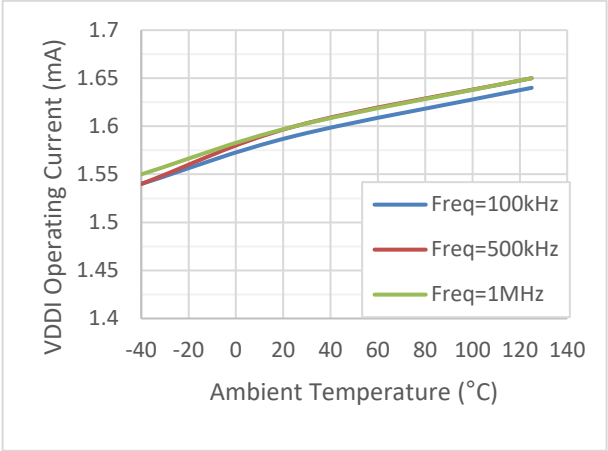


Figure 6.2 VDDI Operating Current vs Temperature

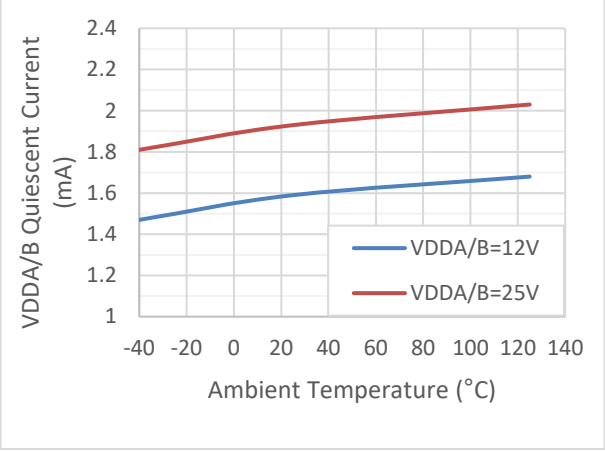


Figure 6.3 VDDA/B Quiescent Current vs Temperature

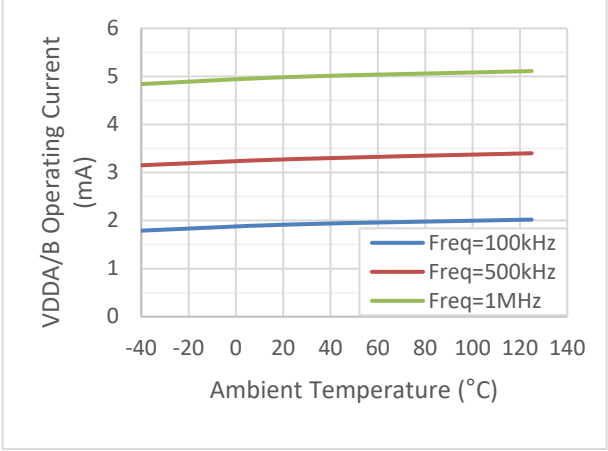


Figure 6.4 VDDA/B Operating Current vs Temperature

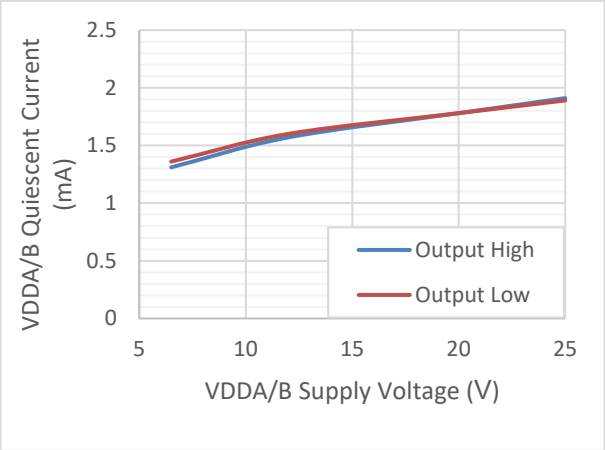


Figure 6.5 VDDA/B Quiescent Current vs Supply Voltage

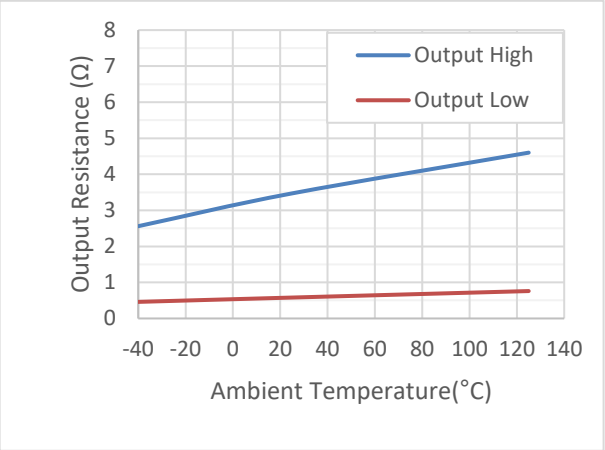


Figure 6.6 Output Resistance vs Temperature

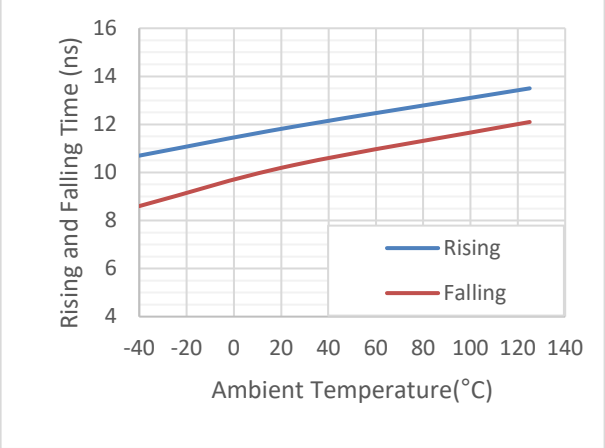


Figure 6.7 Typical Rise Time & Fall Time vs Temperature

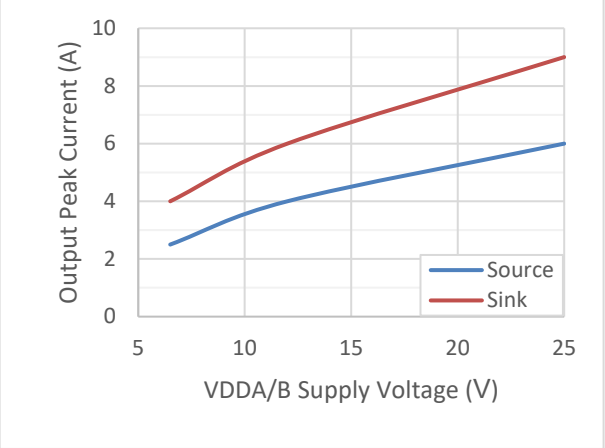


Figure 6.8 Output Peak Current vs VDDA/B Supply Voltage

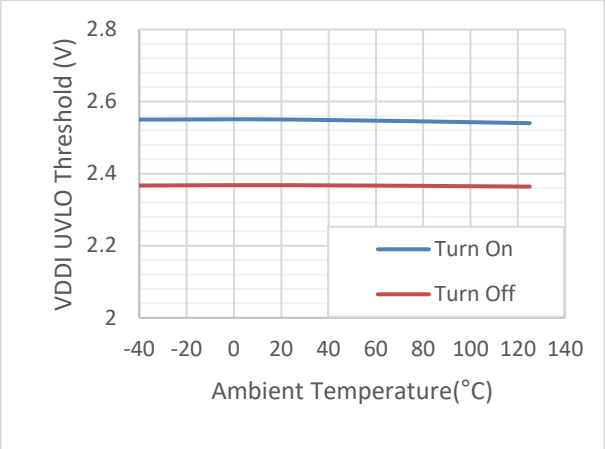


Figure 6.9 VDDI UVLO Threshold vs Temperature

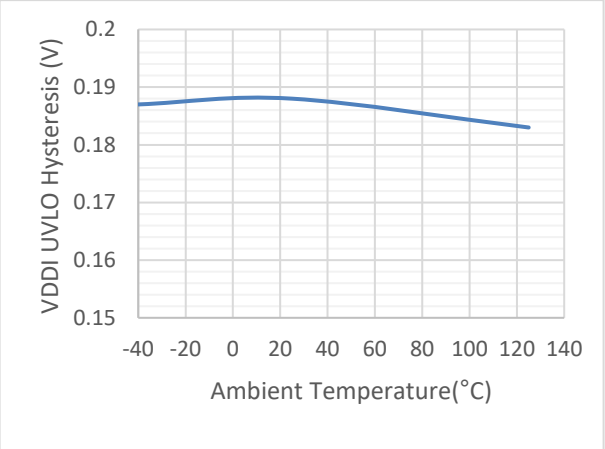


Figure 6.10 VDDI UVLO Hysteresis vs Temperature

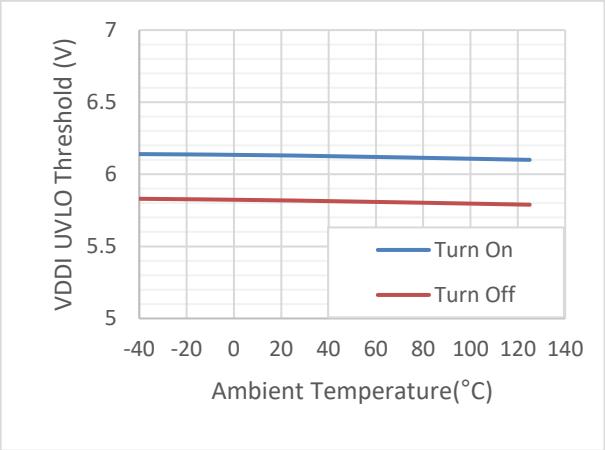


Figure 6.11 6V VDDA/B UVLO Threshold vs Temperature

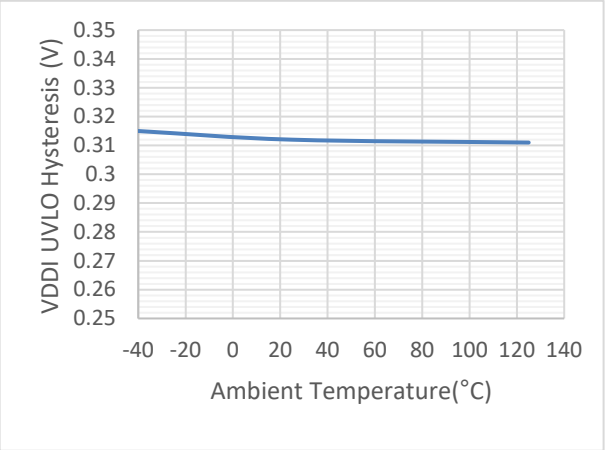


Figure 6.12 6V VDDA/B UVLO Hysteresis vs Temperature

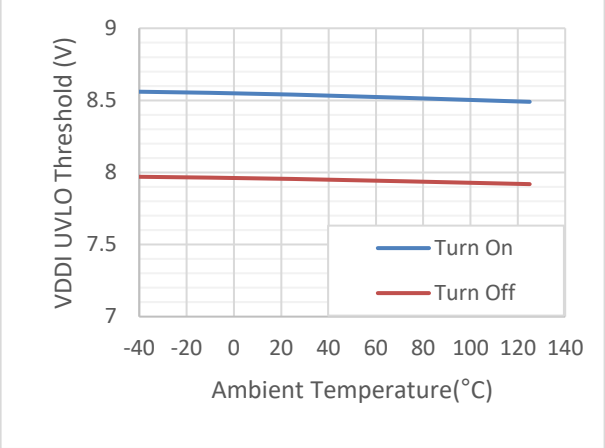


Figure 6.13 8V VDDA/B UVLO Threshold vs Temperature

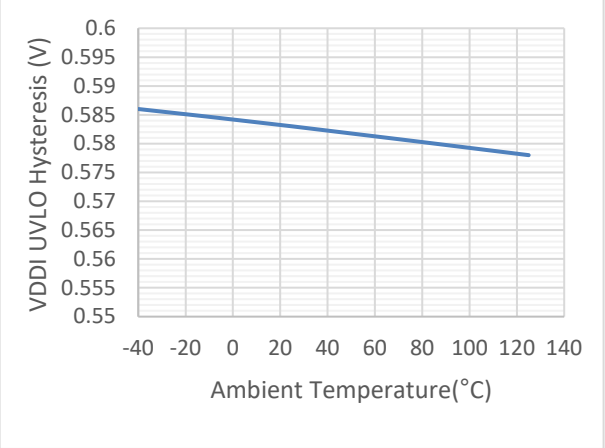


Figure 6.14 8V VDDA/B UVLO Hysteresis vs Temperature

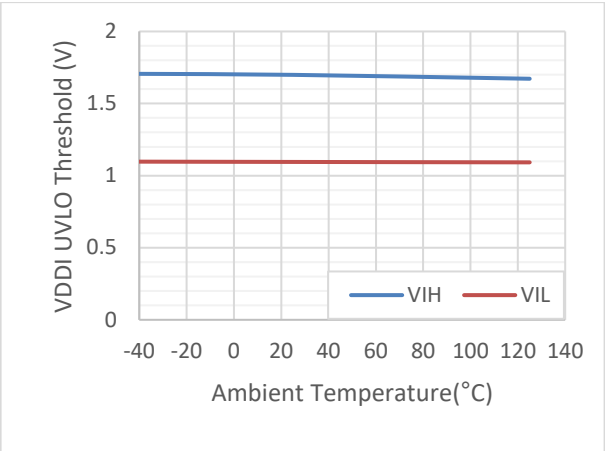


Figure 6.15 INA/INB/DIS Threshold vs Temperature

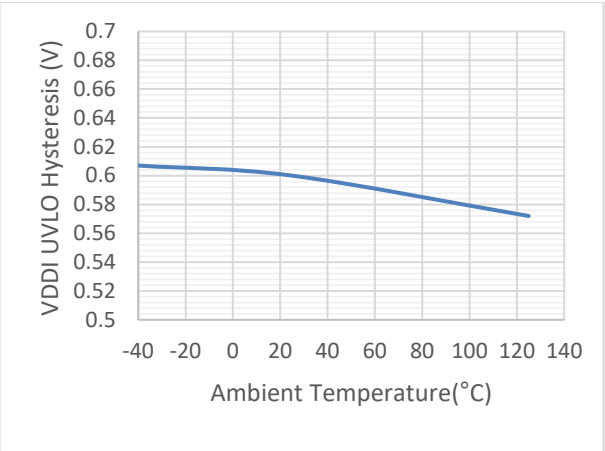


Figure 6.16 INA/INB/DIS Hysteresis vs Temperature

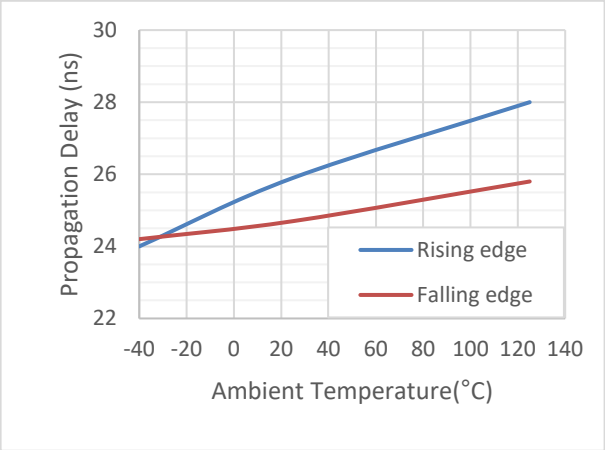


Figure 6.17 Propagation Delay vs Temperature

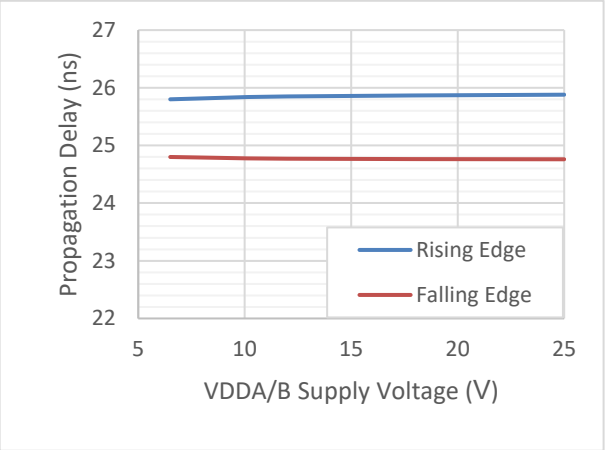


Figure 6.18 Propagation Delay vs VDDA/B

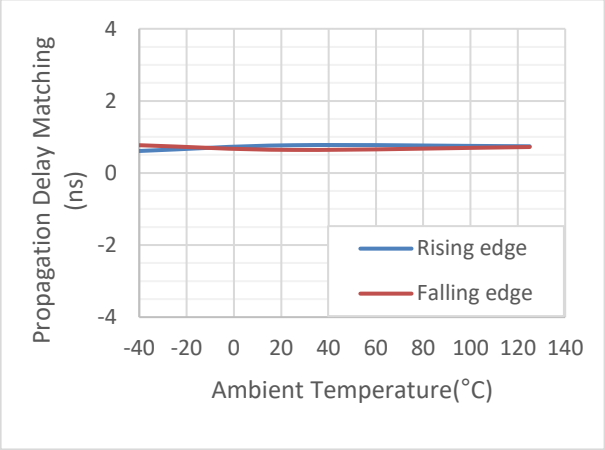


Figure 6.19 Propagation Delay Matching vs Temperature

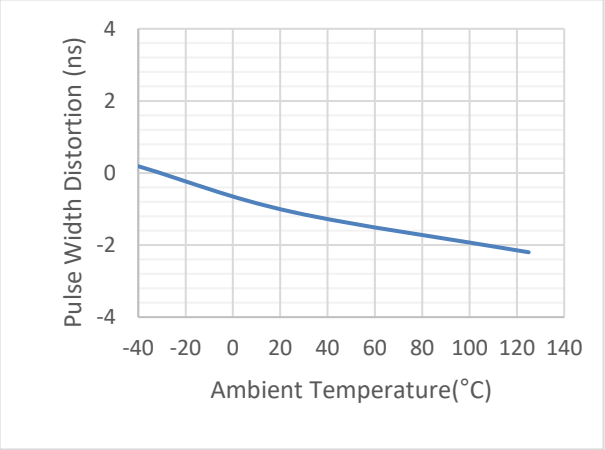


Figure 6.20 Pulse Width Distortion vs Temperature

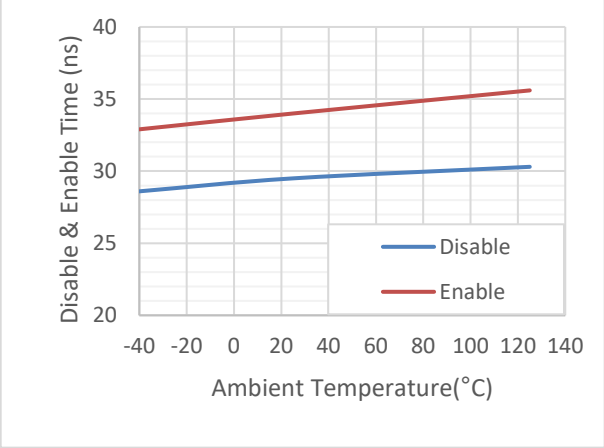


Figure 6.21 Disable & Enable Time vs Temperature

6.4. Parameter Measurement Information

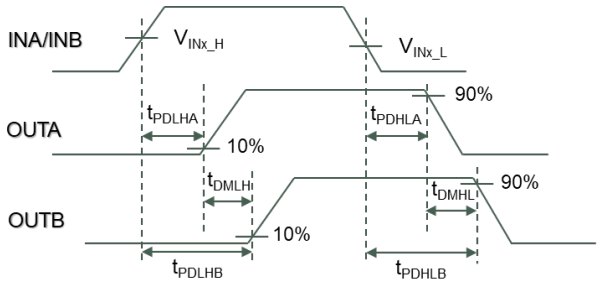


Figure 6.22 Propagation Delay and Channel to Channel Delay Match Time

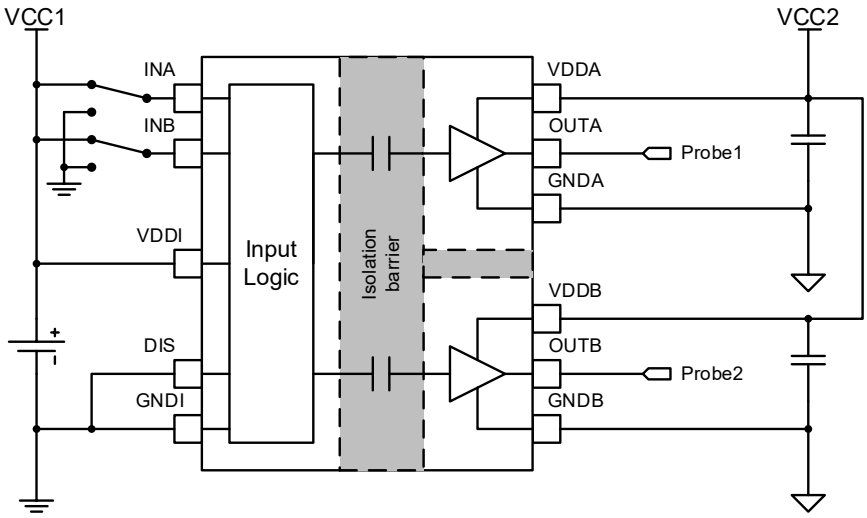


Figure 6.23 Channel to Channel Delay Match Test Circuit

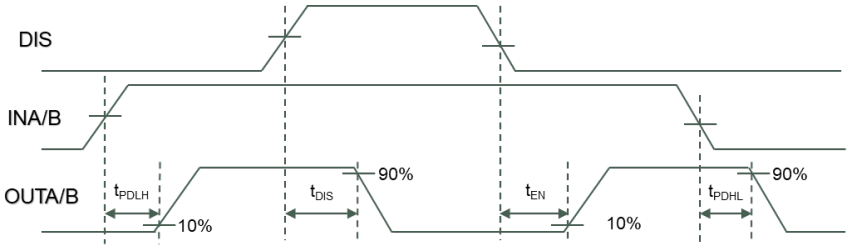


Figure 6.24 Disable Time and Enable Time

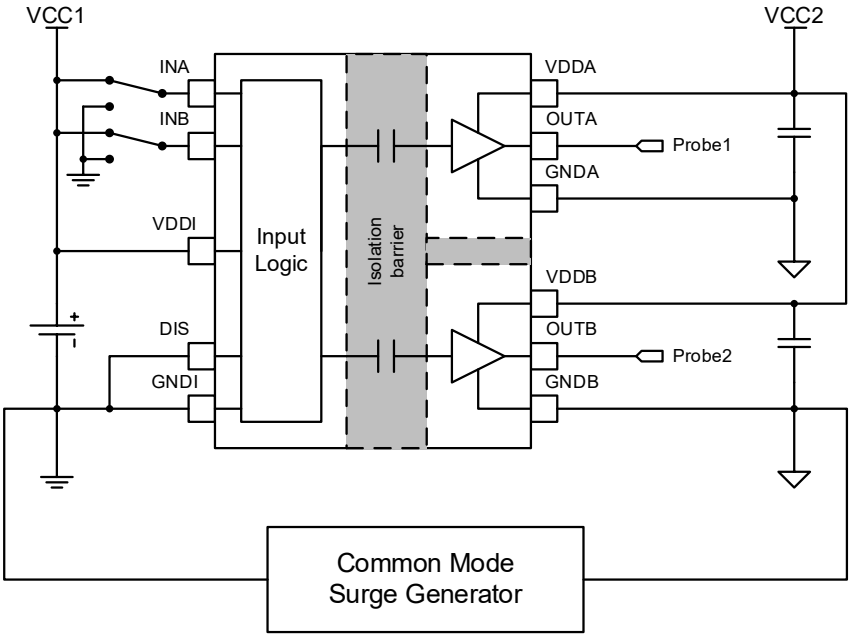


Figure 6.25 Common-Mode Transient Immunity Test Circuit

7. High Voltage Feature Description

7.1. Insulation Characteristics

Description	*Test Condition*	*Symbol*	*Value*			*Unit*
			LGA 13	SOW16/14	SOP16	
Min. External Air Gap (Clearance)		CLR	3.5	8	4	mm
Min. External Tracking (Creepage)		CPG	3.5	8	4	mm
Distance through the Insulation		DTI	32			um
Comparative Tracking Index	DIN EN 60112 (VDE 0303-11)	CTI	>600			V
Material Group	IEC 60664-1		I			
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms		I to III	I to IV	I to IV	
	For Rated Mains Voltage ≤ 300Vrms		I to II	I to IV	I to III	
	For Rated Mains Voltage ≤ 600Vrms		I	I to IV	I to II	
	For Rated Mains Voltage ≤ 1000Vrms		/	I to III	/	
Climatic Category			40/125/21			
Pollution Degree	per DIN VDE 0110, Table 1		2			
Maximum Working Isolation Voltage	AC voltage	V_{IOWM}	560	1000	700	V_{RMS}
	DC voltage		792	1414	990	V_{DC}
Maximum Repetitive Isolation Voltage		V_{IORM}	792	1414	990	V_{peak}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, Vini=V_{IOTM}, t_{ini}=60s, $V_{pd(m)}$=1.2*V_{IORM}, t_m=10s	q_{pd}	/	<5	/	pC
	Method a, after environmental tests subgroup 1, Vini=V_{IOTM}, t_{ini}=60s, $V_{pd(m)}$=1.6*V_{IORM}, t_m=10s		/		/	pC
	Method b, routine test (100% production) and preconditioning (type test); V_{ini}=1.2*V_{IOTM}, t_{ini}=1s, $V_{pd(m)}$=1.875*V_{IORM},t_m=1s（method b1）or $V_{pd(m)}$=Vini, t_m=t_{ini}(method b2)		/		/	pC
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, Vini=V_{IOTM}, t_{ini} =60s, $V_{pd(m)}$=1.2*V_{IORM}, t_m=10s	q_{pd}	<5	/	<5	pC

Description	Test Condition	Symbol	Value			Unit
	Method a, after environmental tests subgroup 1, Vini=V_{IOTM}, t_{ini}=60s, $V_{pd(m)}$=1.3*V_{IORM}, t_m=10s			/		pC
	Method b, routine test (100% production) and preconditioning (type test); V_{ini}=1.2*V_{IOTM}, t_{ini}=1s $V_{pd\ (m)}$=1.5*V_{IORM}, t_m=1s(method b1)or $V_{pd(m)}$=Vini, t_m=t_{ini}(method b2)			/		pC
Maximum Transient Isolation Voltage	t = 60 sec	V_{IOTM}	3535	8000	4242	V
Maximum impulse voltage	Tested in air, 1.2/50μs waveform per IEC62368-1	V_{imp}	2000	6000	3500	V
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50μs waveform, VIOSM≥VIMP × 1.3	V_{IOSM}	3500	10000	6000	V
Isolation Resistance	V_{IO} = 500 V, Tamb = 25 °C	R_{IO}	>10^{12}			Ω
	V_{IO} = 500 V, T_{amb} = T_S		>10^{9}			Ω
	V_{IO} = 500 V, 100 °C ≤ T_{amb} ≤ 125 °C		>10^{11}			Ω
Isolation Capacitance	f = 1MHz	C_{IO}	1.2			pF
Insulation Specification per UL1577						
Withstand Isolation Voltage	V_{TEST} = 1.2 × V_{ISO}, t = 1 sec, 100% production test	V_{ISO}	2500	5700	3000	V_{rms}

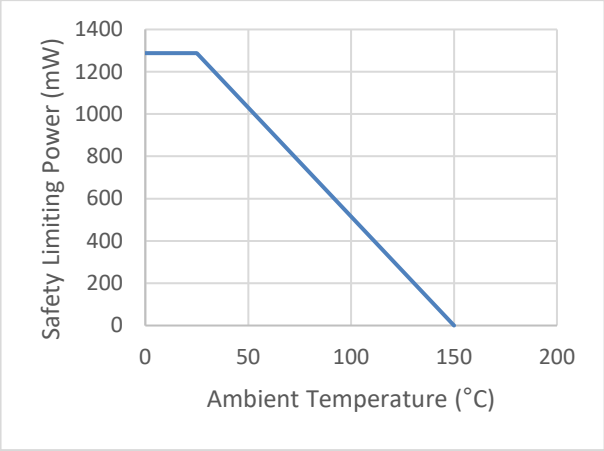
7.2. Safety-Limiting Values

Reinforced isolation safety-limiting values as outlined in VDE-0884-11 of NSI6622x-xSWxR (SOW16/SOW14)

Description	Test Condition	Side	Value	Unit
Safety Supply Power	$R_{θJA}$ = 97 °C/W[1)], T_J = 150 °C, T_A = 25 °C	Input	12	mW
		Driver A, Driver B	638	mW
		Total	1288	mW
Safety Supply Current	$R_{θJA}$ = 97 °C/ W[1)], VDDA/B = 12V, T_J = 150 °C, T_A = 25 °C	Driver A, Driver B	53.1	mA
	$R_{θJA}$ = 97 °C/ W[1)], VDDA/B = 25V, T_J = 150 °C, T_A = 25 °C	Driver A, Driver B	25.5	mA
Safety Temperature[2)]			150	°C

1) Calculate with the junction-to-air thermal resistance, $R_{θJA}$, of SOW16/SOW14 package (***Thermal Information Table***) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.

2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.



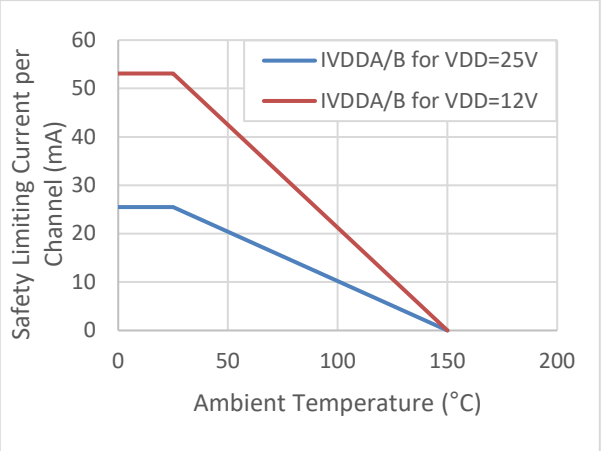


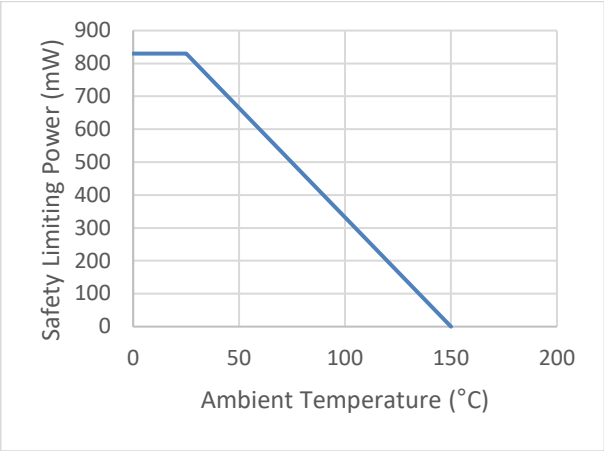
Figure 6.26 NSI6622x-DSWR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

Basic isolation safety-limiting values as outlined in VDE-0884-11 of NSI6622x-xSPNR (SOP16)

Description	*Test Condition*	*Side*	*Value*	*Unit*
Safety Supply Power	$R_{\theta JA}$ = 150.5 °C/W[1)], T_J = 150 °C, T_A = 25 °C	Input	12	mW
		Driver A, Driver B	409	mW
		Total	830	mW
Safety Supply Current	$R_{\theta JA}$ = 150.5 °C/ W[1)], VDDA/B = 12V, T_J = 150 °C, T_A = 25 °C	Driver A, Driver B	34.0	mA
	$R_{\theta JA}$ = 150.5 °C/ W[1)], VDDA/B = 25V, T_J = 150 °C, T_A = 25 °C	Driver A, Driver B	16.3	mA
Safety Temperature[2)]			150	°C

1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOP16 package (***Thermal Information Table***) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.

2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.



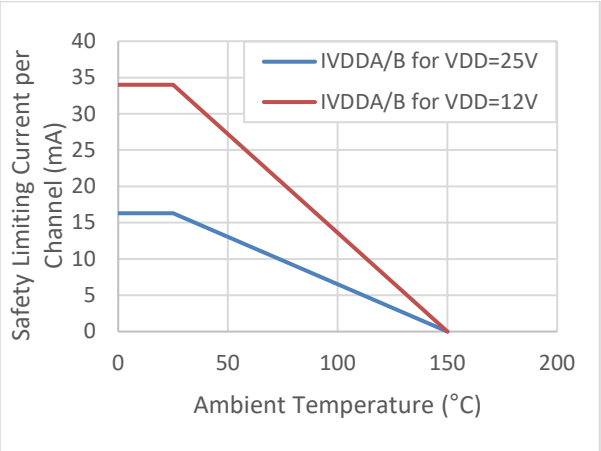


Figure 6.27 NSI6622x-DSWR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

Basic isolation safety-limiting values as outlined in VDE-0884-11 of NSI6622x-xLAR (LGA13)

Description	Test Condition	Side	Value	Unit
Safety Supply Power	$R_{\theta JA}$ = 209.5 °C/W[1)], T_J = 150 °C, T_A = 25 °C	Input	12	mW
		Driver A, Driver B	293	mW
		Total	598	mW
Safety Supply Current	$R_{\theta JA}$ = 209.5 °C/ W[1)], VDDA/B = 12V, T_J = 150 °C, T_A = 25 °C	Driver A, Driver B	24.4	mA
	$R_{\theta JA}$ = 209.5 °C/ W[1)], VDDA/B = 25V, T_J = 150 °C, T_A = 25 °C	Driver A, Driver B	11.7	mA
Safety Temperature[2)]			150	°C

1) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of LGA13 package (***Thermal Information Table***) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.

2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

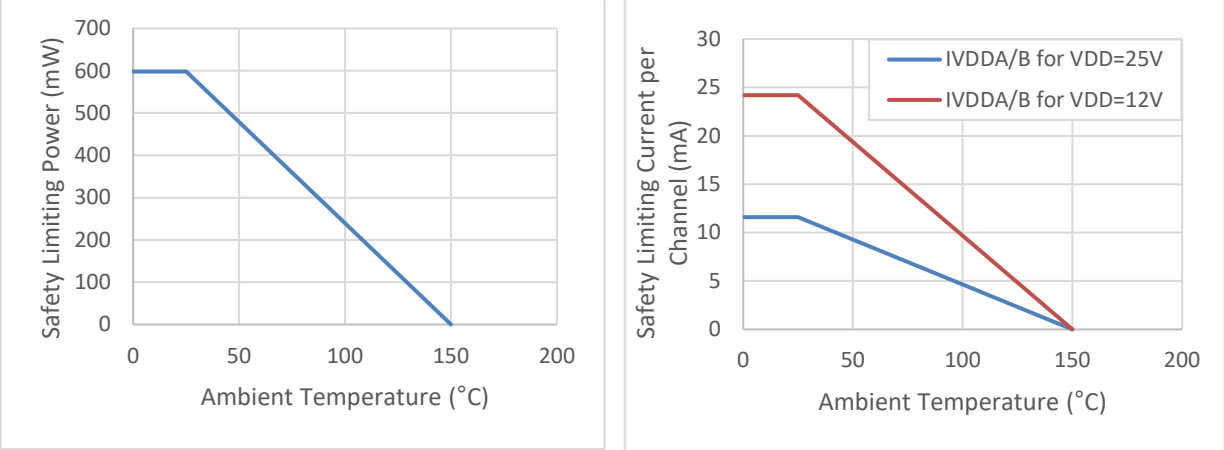


Figure 6.28 NSI6622x-DLAR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

7.3. Safety-Related Certifications

The NSI6622x-DSWxR(SOW16/SOW14) are approved or pending approval by the organizations listed in table.

CUL		VDE	CQC
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11: 2017-01	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 5700Vrms Isolation voltage	Single Protection, 5700Vrms Isolation voltage	Reinforced insulation at V_{IORM}=1414V_{PEAK} V_{IOSM}=6250V_{PEAK} V_{IOTM}=8000V_{PEAK}	Reinforced insulation
E500602	E500602	Certification No. 40052820	CQC20001264939

The NSI6622x-DSPNR(SOP16) are approved or pending approval by the organizations listed in table.

CUL		*VDE*	*CQC*
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 3000Vrms Isolation voltage	Single Protection, 3000Vrms Isolation voltage	Basic insulation at V_{IORM}=990V_{PEAK} V_{IOSM}=6000V_{PEAK} V_{IOTM}=4242V_{PEAK}	Basic insulation
E500602	E500602	Certification No.40050121	CQC21001289931

The NSI6622x-DLAR(LGA13) are approved or pending approval by the organizations listed in table.

CUL		*VDE*	*CQC*
UL1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11: 2017-01	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 2500Vrms Isolation voltage	Single Protection,2500Vrms Isolation voltage	Basic Insulation at V_{IORM}=792V_{PEAK} V_{IOSM}=3500V_{PEAK} V_{IOTM}=3535V_{PEAK}	Basic insulation
E500602	E500602	Certification No.40057024	CQC21001289933

8. Function Description

8.1. Overview

NSI6622 is a high reliability dual channel isolated gate driver which could be designed in variety switching power and motor drive topologies. NSI6622 has some useful protections, such as under voltage lock-out (UVLO) for both input and output supply, a disable pin, default low output as input is floating. The functional circuit block diagram is shown as below:

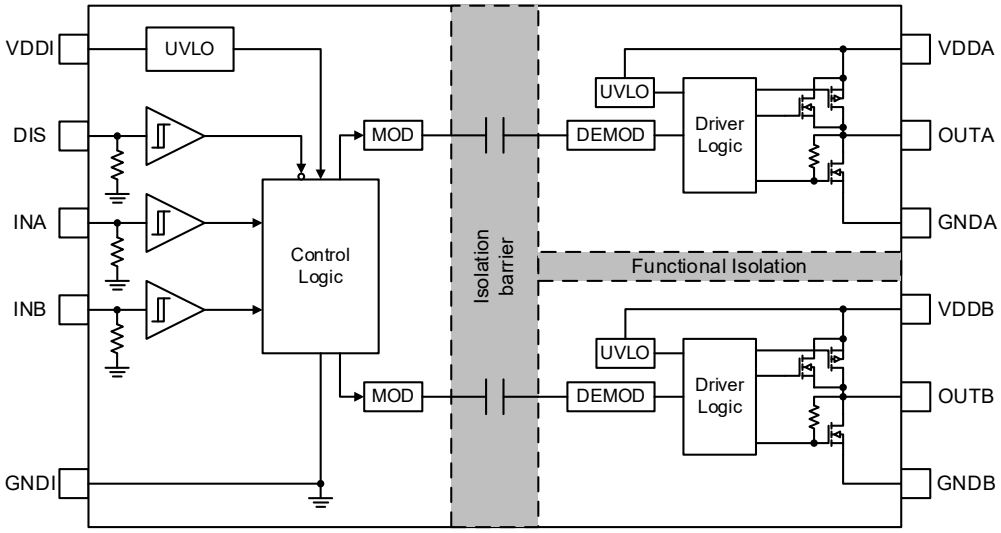


Figure 8.1 Functional Block Diagram

8.2. Under Voltage Lock Out (UVLO)

The NSI6622 has an internal under voltage lock out (UVLO) protection on both input and output supply circuit blocks. The driver output is held low by an active clamp circuit when the supply voltage of VDDI or VDDA/VDDB is lower than V_{VDD_ON} at power-up status or lower than V_{VDD_OFF} after power-up, regardless of the status of the input pins.

The VDDI and VDDA/B ULVO protections have hysteresis (V_{VDD_HYS}) to prevent chatter noise from VDD supply and allow small drops in supply power which are usually happened in startup.

8.3. Input and Output Logic Table

When the device is power up, setting the DIS pin high can shut down both outputs simultaneously. Left open or grounding the DIS pin can allow the device operating normally.

Table 8.1 Output status vs. Input and Power status

VDDI status	*VDDA/B status*	*DIS*	*IN*		*OUT*		*NOTE[1)]*
			A	*B*	*A*	*B*	
PU	PU	L or O	L	H	L	H	
PU	PU	L or O	H	L	H	L	
PU	PU	L or O	H	H	H	H	
PU	PU	L or O	L	L	L	L	
PU	PU	L or O	O	O	L	L	
PU	PU	H	X	X	L	L	
PU	PD	X	X	X	L	L	
PD	PU	X	X	X	L	L	

1) PD= Power Down; PU= Power Up; H= Logic High; L= Logic Low; O= Left Open; X= Irrelevant.

8.4. ESD Protection

Figure 8.2 shows the multiple diodes involved in the ESD protection part of NSI6622.

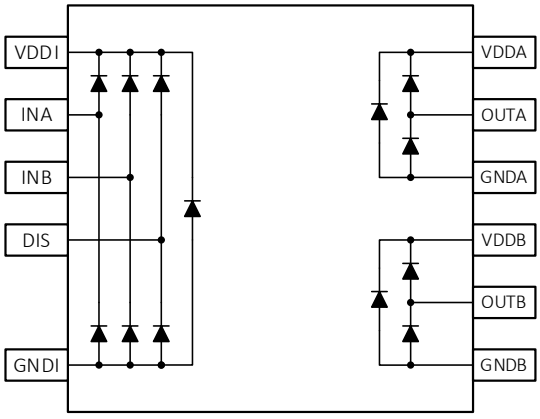


Figure 8.2 ESD Structure

9. Application Note

9.1. Typical Application Circuit

The circuit shows a typical half-bridge configuration by using the driver NSI6622 which could be used in several popular power converter topologies such as half-bridge/full bridge/LLC isolated topologies, buck-boost topologies, and 3-phase motor drive applications.

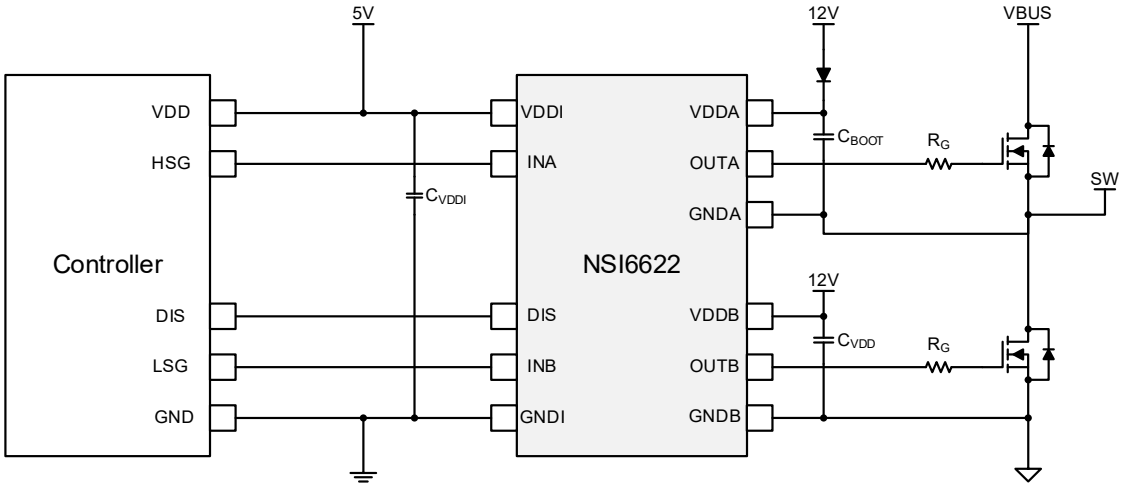


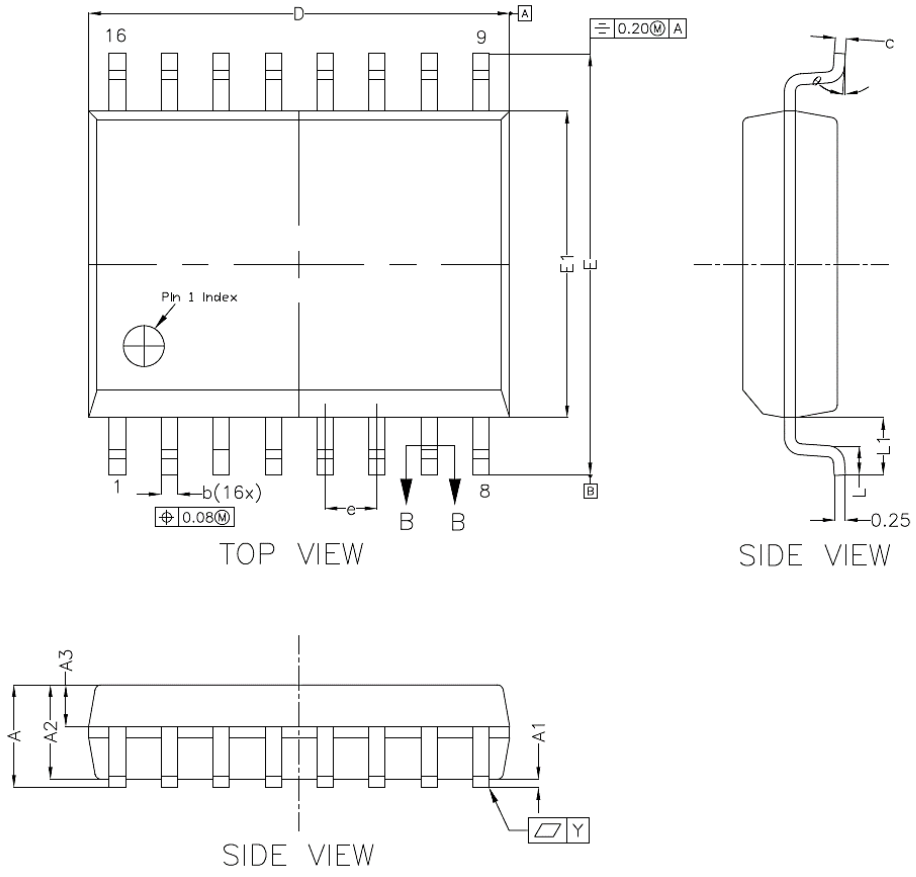
Figure 9.1 Typical Half-Bridge Application Schematic

9.2. PCB Layout

PCB layout is important to get optimal performance. Some key guidelines are given as below:

- Low-ESR and low-ESL bypass capacitors should be placed close to the device between pin VDDI to GND and pin VDDA/B to GNDA/B.
- There is high frequency switching current that charges and discharges the gate of external power transistor, leading to EMI and ring issues. The parasitic inductance of this loop should be minimized, by decreasing loop area and placing NSI6622 close to power transistor.
- Large amount of copper should be placed at VDDA/B pin and GNDA/B pin for thermal dissipation.
- To ensure isolation performance between primary and secondary side, the space under the device should keep free from any plane, trace, pad or via.

10. Package information



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.10	---	030
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	---	0.43
c	0.23	---	0.32
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 bsc		
L1	1.40 bsc		
L	0.55	---	0.85
Y	---	0.10	---
θ	0°	---	8°

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 10.1 SOW16 Package Shape and Dimension

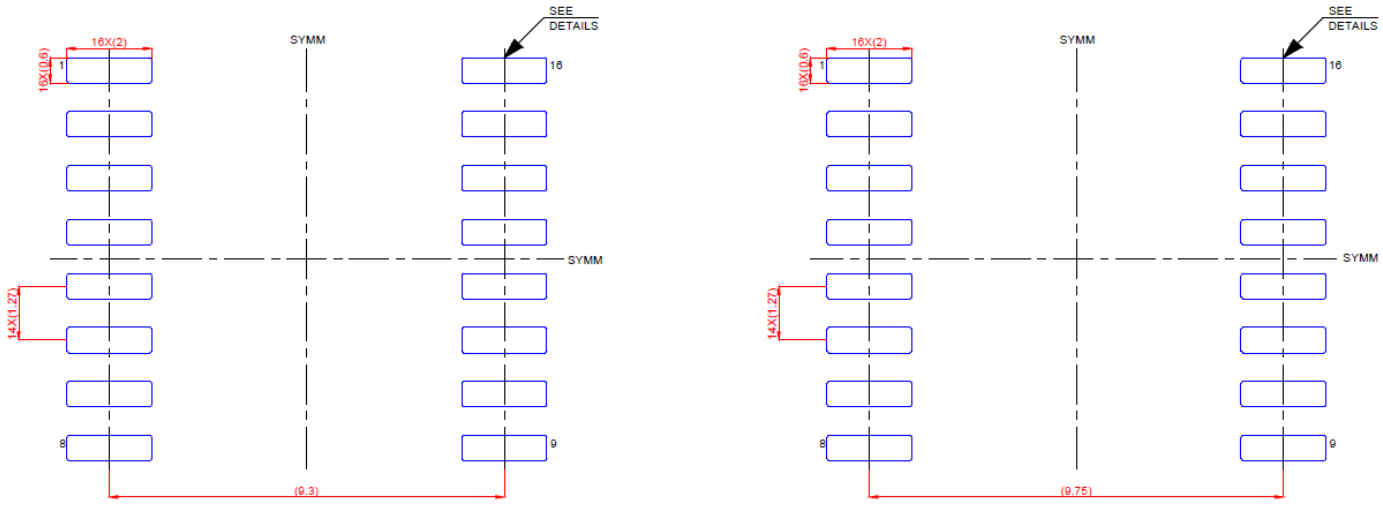
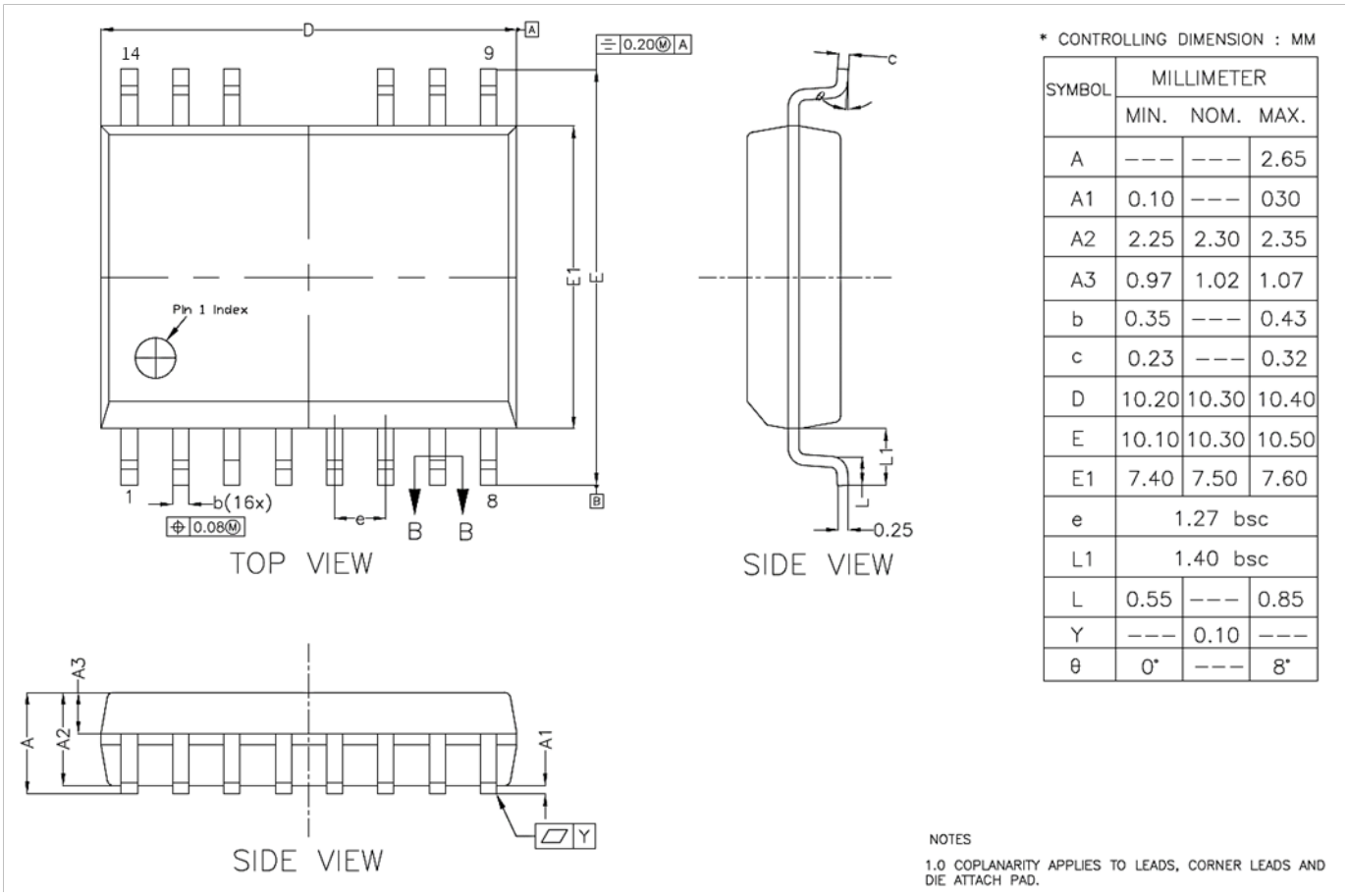


Figure 10.2 SOW16 Package Board Layout Example(mm)



SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.10	---	030
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	---	0.43
c	0.23	---	0.32
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 bsc		
L1	1.40 bsc		
L	0.55	---	0.85
Y	---	0.10	---
θ	0°	---	8°

Figure 10.3 SOW14 Package Shape and Dimension

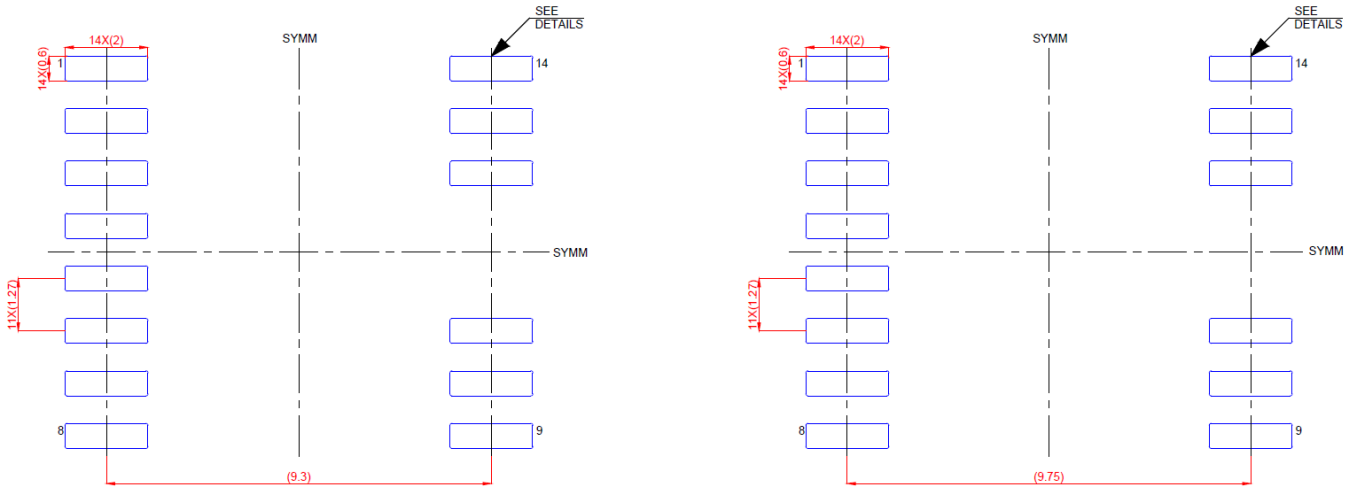
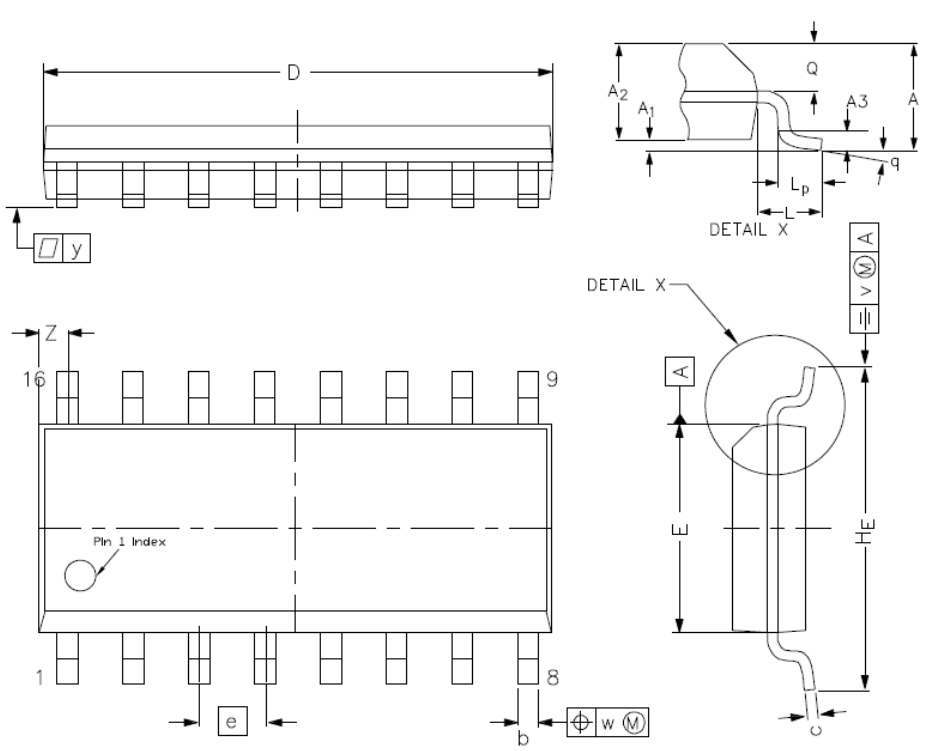


Figure 10.4 SOW14 Package Board Layout Example(mm)



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	1.75	---	---	0.069
A1	0.10	---	0.25	0.004	---	0.010
A2	1.25	---	1.45	0.049	---	0.057
b	0.36	---	0.49	0.014	---	0.019
c	0.19	---	0.25	0.007	---	0.010
D	9.80	9.90	10.0	0.386	0.390	0.394
E	3.80	3.90	4.00	0.150	0.154	0.158
HE	5.80	---	6.20	0.228	---	0.244
Q	0.60	---	0.70	0.024	---	0.028
e	1.27 bsc			0.050 bsc		
L	1.05 bsc			0.041 bsc		
Lp	0.40	---	1.00	0.016	---	0.039
Y	---	0.10	---	---	0.004	---
A3	---	0.25	---	---	0.010	---
Z	0.30		0.70	0.012		0.028
θ	0°	---	8°	0°	---	8°

Figure 10.5 SOP16 Package Shape and Dimension

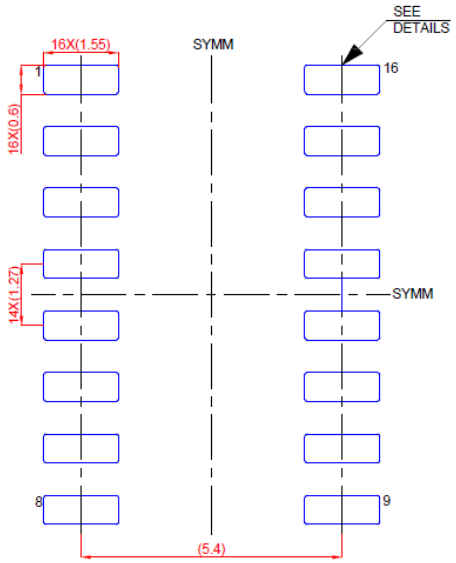
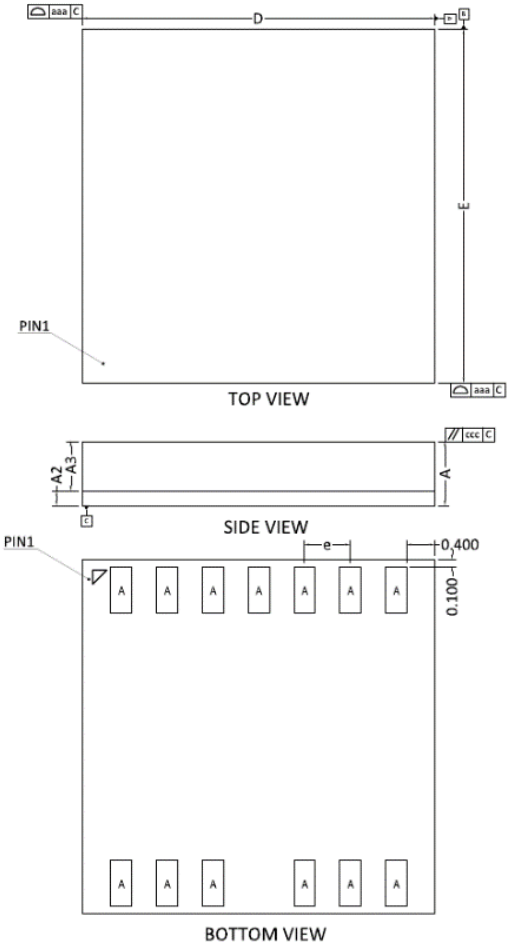


Figure 10.6 SOP16 Package Board Layout Example(mm)



MILLIMETER			
SYMBOL	MIN	NOR	MAX
A	0.83	0.91	0.99
A2	0.18	0.21	0.24
A3	0.65	0.70	0.75
D	4.90	5.00	5.10
E	4.90	5.00	5.10
e	0.65 BSC		
aaa	0.10		
ccc	0.05		

Figure 10.7 LGA13 Package Shape and Dimension

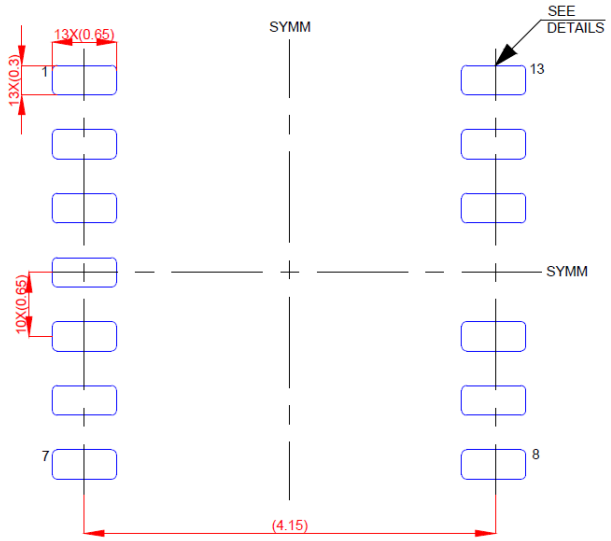


Figure 10.8 LGA13 Package Board Layout Example(mm)

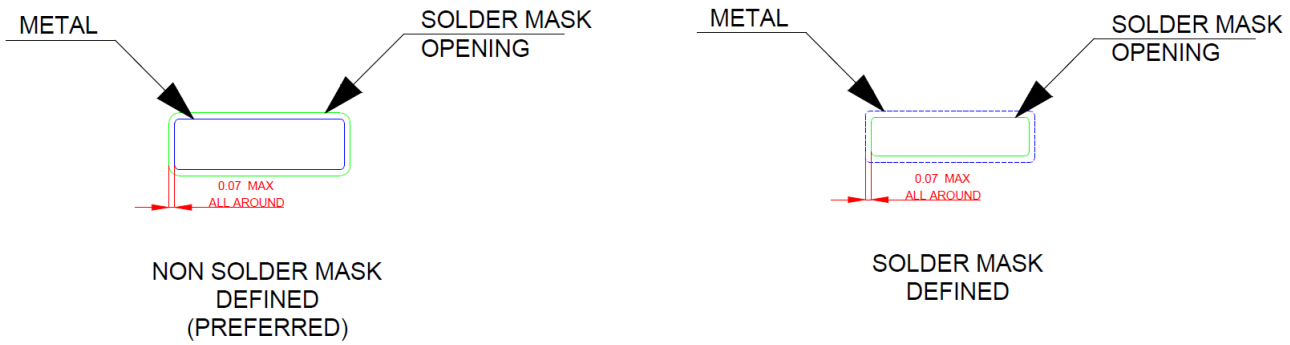


Figure 10.9 Solder Mask Details(mm)

11. Ordering Information

Part No.	*Isolation Rating(kV_{RMS})*	*Driver-side UVLO TYP.*	*Temperature*	*Auto-motive*	*Package Type*	*MSL*	*SPQ*
NSI6622A-DSWR	5.7	6V	-40 to 125℃	NO	SOW16	2	1000
NSI6622A-DSWKR	5.7	6V	-40 to 125℃	NO	SOW14	2	1000
NSI6622A-DSPNR	3.0	6V	-40 to 125℃	NO	SOP16	1	2500
NSI6622A-DLAR	2.5	6V	-40 to 125℃	NO	LGA13	3	3000
NSI6622B-DSWR	5.7	8V	-40 to 125℃	NO	SOW16	2	1000
NSI6622B-DSWKR	5.7	8V	-40 to 125℃	NO	SOW14	2	1000
NSI6622B-DSPNR	3.0	8V	-40 to 125℃	NO	SOP16	1	2500
NSI6622B-DLAR	2.5	8V	-40 to 125℃	NO	LGA13	3	3000
NSI6622C-DSWR	5.7	13V	-40 to 125℃	NO	SOW16	2	1000
NSI6622C-DSWKR	5.7	13V	-40 to 125℃	NO	SOW14	2	1000
NSI6622C-DSPNR	3.0	13V	-40 to 125℃	NO	SOP16	1	2500
NSI6622C-DLAR	2.5	13V	-40 to 125℃	NO	LGA13	3	3000

12. Tape and Reel Information

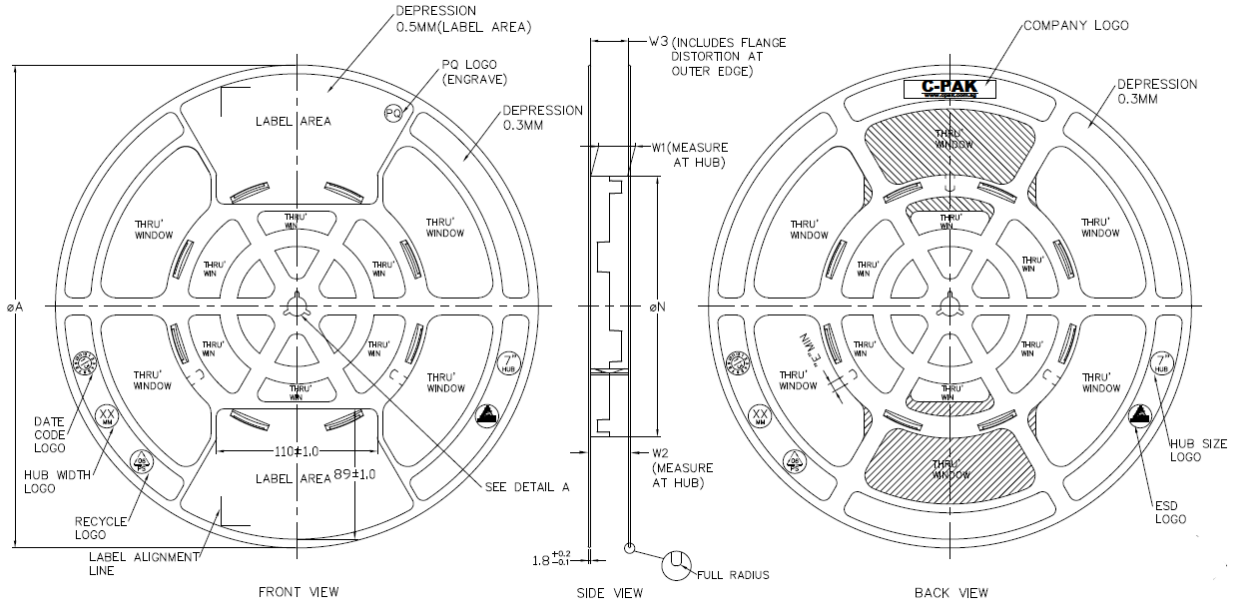


Figure 12.1 Tape Information

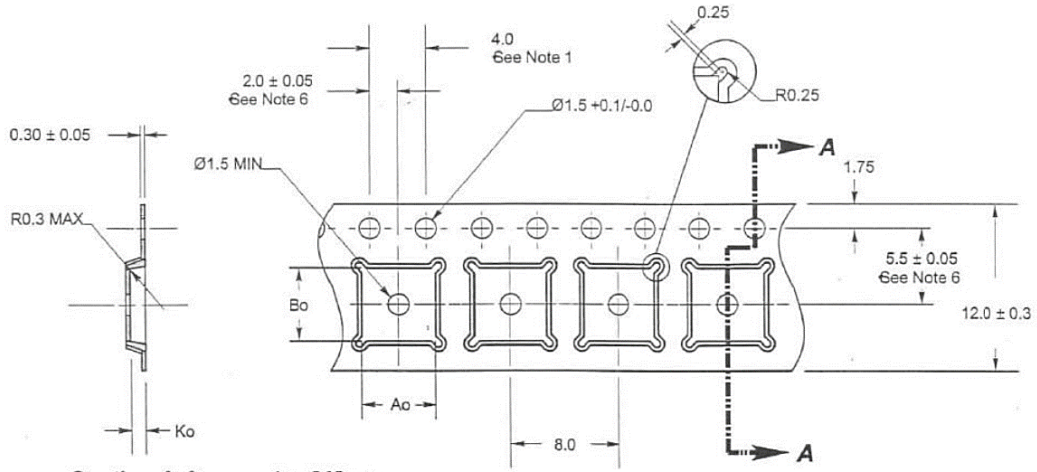
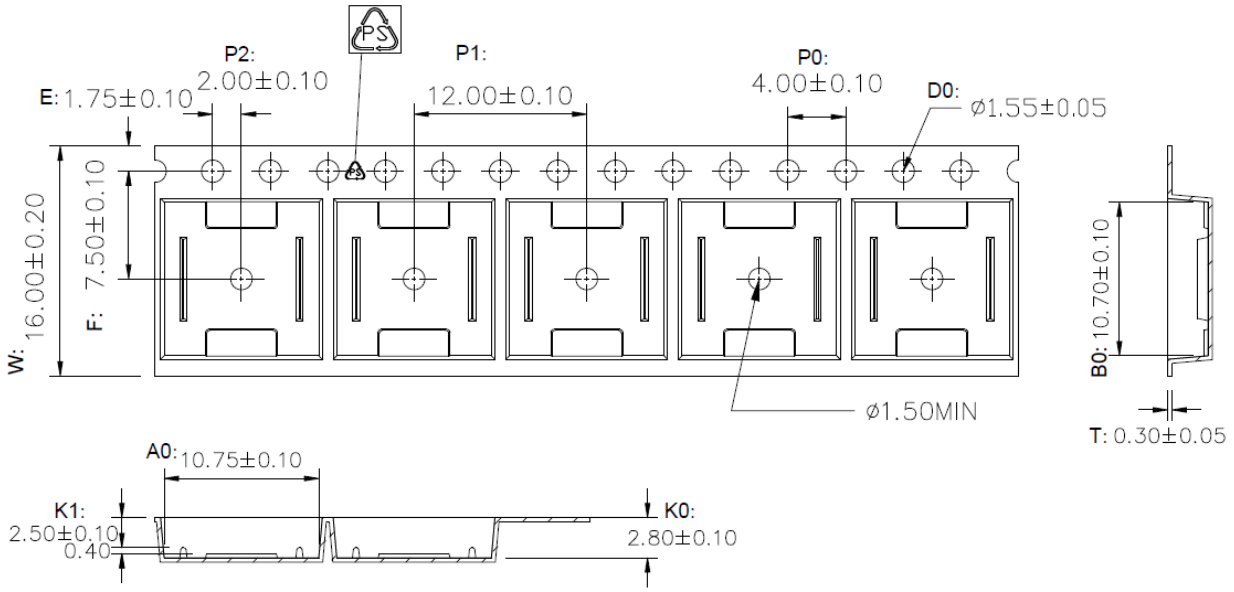
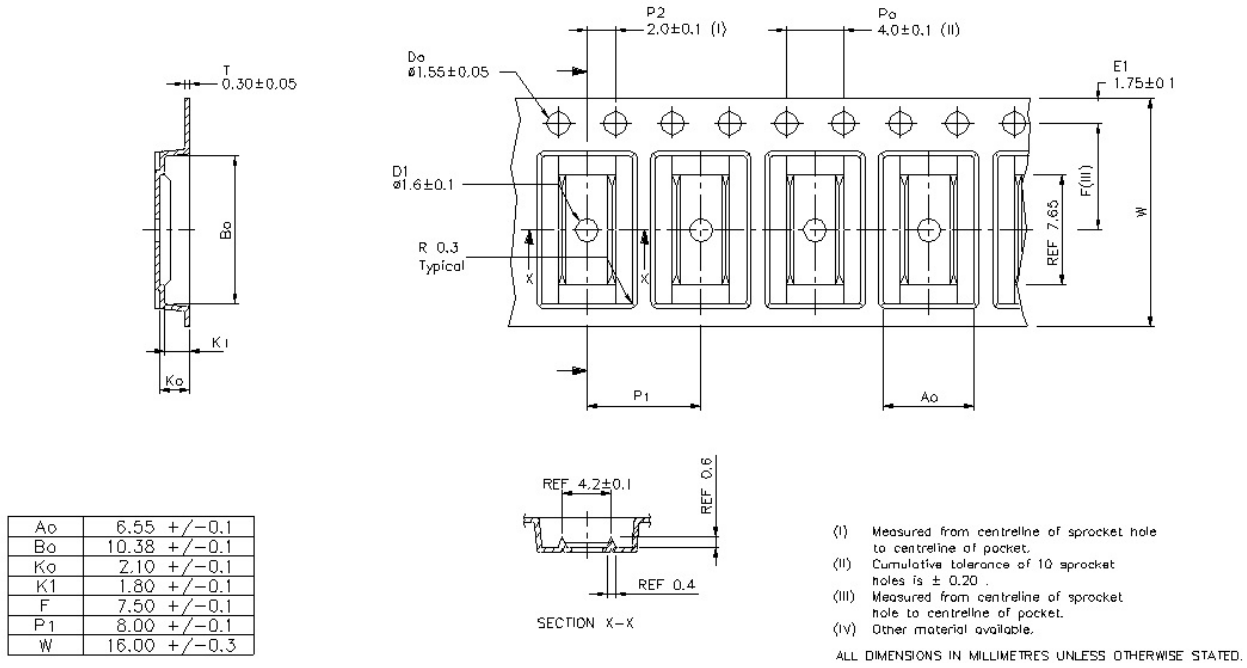


Figure 12.2 LGA13 Reel Information



1. 10 sprocket hole pitch cumulative tolerance ±0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy .
4. All dimensions meet EIA-481 requirements.
5. Thickness : 0.30±0.05mm.
6. Packing length per 22" reel : 378 Meters.(N=122)
7. Component load per 13" reel : 1000 pcs.

Figure 12.3 SOW16/SOW14 Reel Information



Ao	6.55 +/-0.1
Bo	10.38 +/-0.1
Ko	2.10 +/-0.1
K1	1.80 +/-0.1
F	7.50 +/-0.1
P1	8.00 +/-0.1
W	16.00 +/-0.3

Figure 12.4 SOP16 Reel Information

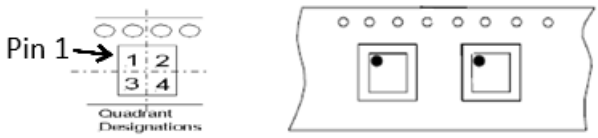


Figure 12.5 Quadrant Designation for Pin1 Orientation in Tape

13. Revision History

Revision	Description	Date
1.0	Initial version	2021/3/12
1.1	Increase SOP16 and LGA13 packages information.	2021/8/18
1.2	1. Update Figure 1.3 Description. 2. Remove junction temperature of recommended operating conditions	2023/6/13
1.3	1. Add RoHS & REACH Qualified in key features. 2.Modify device name from NSi6622 to NSI6622 3.Modify Ordering Information 4.Update High Voltage Feature Description 5.Modify SOP16(150mil) to SOP16, SOP16/SOP14(300mil) to SOW16/SOW14 6.Change the description of ESD Ratings	2023/9/19

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