

H2M065B100

Silicon Carbide MOSFET
N-CHANNEL ENHANCEMENT MODE

Features

- Low On-Resistance and High Current Density
- Low Capacitance for High Frequency Operation
- Ultra-high Avalanche Ruggedness
- Positive Temperature Coefficient Device
- RoHS Compliant and Halogen Free

Benefits

- Higher System Efficiency
- Increase Parallel Device Convenience
- Capable of 175°C High T_j Application
- Allow High Frequency Operation
- Realize Compact and Lightweight Systems

Applications

- Switching Mode Power Supply
- DC/DC Converters, UPS, and PFC
- EV Charging Station
- Motor Drives
- Power Inverters
- Solar/Wind Renewable Energy

Absolute Maximum Ratings ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Value	Unit
Drain – Source Voltage	$V_{DS,max}$	$V_{GS}=0V, I_{DS}=100\mu A$	650	V
Continuous Drain Current	I_D	$V_{GS}=20V, T_c=25^\circ\text{C}$	32	A
		$V_{GS}=20V, T_c=100^\circ\text{C}$	24	
Pulse Drain Current	$I_{D,pulse}$	t_{PW} limitation per Fig.15	114	
Power Dissipation	P_D	$T_c=25^\circ\text{C}$	176	W
Recommend Gate Source Voltage	$V_{GS,op}$	Static, recommended DC operating values	-5 to 20	V
Maximum Gate Source Voltage	$V_{GS,max}$	Transient operating limit (AC $f > 1\text{Hz}$, duty cycle $< 1\%$)	-10 to 25	
Junction & Storage Temperature	T_j, T_{stg}		-55 to 175	$^\circ\text{C}$
Soldering Temperature	T_L		260	
Mounting Torque	M_D	M3 or 6-32 screw	1.0	Nm

Thermal Resistance

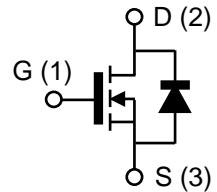
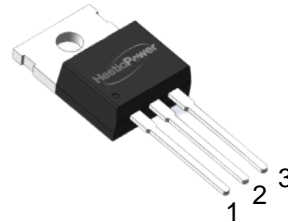
Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal Resistance, Junction to Case	$R_{\theta,jc}$		0.85		$^\circ\text{C/W}$

Product Summary

V_{DS}	650V
$I_D(@25^\circ\text{C})$	32A
$R_{DS(on)}$	100mΩ



Circuit Diagram



Part Number	Package	Marking
H2M065B100	TO-220-3L	H2M065B100

Description

The H2M065B100 650V, 100mΩ silicon carbide power MOSFET is an N-channel enhancement mode device. Exploiting the outstanding wide bandgap material properties, this device shows high current density and great switching behavior. Thanks for the excellent thermal conductivity and many advantages of SiC, this device significantly improved in thermal capability and temperature independent switching behavior.

Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_{DS}=100\mu A$	650			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=10V, I_{DS}=10mA$	1.5	2.7	4.5	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=650V, V_{GS}=0V$		<1	50	μA
		$V_{DS}=650V, V_{GS}=0V$ $T_j=175^\circ\text{C}$		10		
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=20V, V_{DS}=0V$			250	nA
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=20V, I_{DS}=10A$		100	130	mΩ
		$V_{GS}=20V, I_{DS}=10A$, $T_j=175^\circ\text{C}$		122		
Transconductance	g_{fs}	$V_{DS}=17V, I_{DS}=20A$		7.6		S
Input Capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=400V$ $f=1MHz, V_{AC}=25mV$		1754		pF
Output Capacitance	C_{oss}			118		
Reverse Transfer Capacitance	C_{rss}			15		
Effective Output Capacitance, Energy Related	$C_{o(er)}$		$V_{GS}=0V$, $V_{DS}=0$ to 400V		129	
Effective Output Capacitance, Time Related	$C_{o(tr)}$	$I_D=const.$, $V_{GS}=0V$, $V_{DS}=0$ to 400V		167		
Turn On Delay Time	$t_{d(on)}$	$V_{DS}=400V, V_{GS}=-5/+20V$, $I_D=10A, R_L=40\Omega$, $R_{G(ext)}=2.7\Omega$		17		ns
Rise Time	t_r			28		
Turn Off Delay Time	$t_{d(off)}$			24		
Fall Time	t_f			40		
C_{oss} Stored Energy	E_{oss}	$V_{GS}=0V, V_{DS}=400V$ $f=1MHz, V_{AC}=25mV$		10		μJ
Turn-on Switching Energy	E_{on}	$V_{DS}=400V, V_{GS}=0/+20V$, $I_D=10A$,		78		
Turn-off Switching Energy	E_{off}	$R_{G(ext)}=2.7\Omega$		9		
Internal Gate Resistance	$R_{G(int.)}$	$f=1MHz, V_{AC}=25mV$		1.4		Ω

Built-in SiC Diode Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Typ.	Unit
Inverse Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_{SD}=3A$	2.9	V
Continuous Diode Forward Current	I_S	$V_{GS}=0V, T_c=25^\circ\text{C}$	30	A
Reverse Recovery Time	t_{rr}	$V_{GS}=0V$,	53	ns
Reverse Recovery Charge	Q_{rr}	$I_{SD}=10A, V_{DS}=400V$,	59	nC
Peak Reverse Recovery Current	I_{rrm}	$di/dt=300A/\mu s$	2.2	A

Gate Charge Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Value	Unit
Gate to Source Charge	Q_{GS}	$V_{DS}=400V$, $V_{GS}=-5/+20V$, $I_D=10A$	26	nC
Gate to Drain Charge	Q_{GD}		27	
Total Gate Charge	Q_G		90	
Gate plateau voltage	V_{pl}		9.2	V

Typical Device Performance

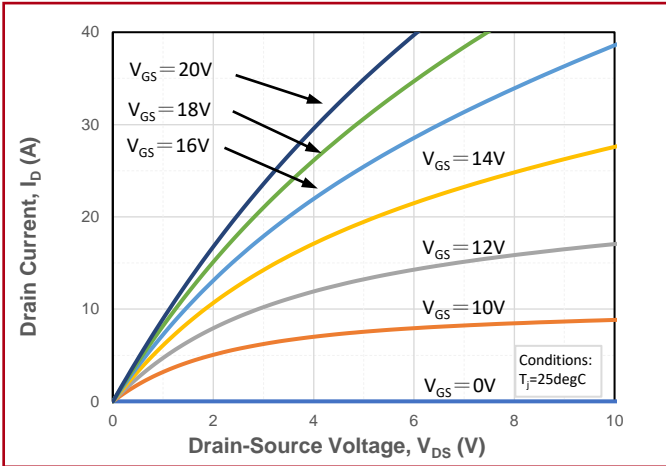


Fig.1 Forward Output Characteristics at $T_j = 25^\circ\text{C}$

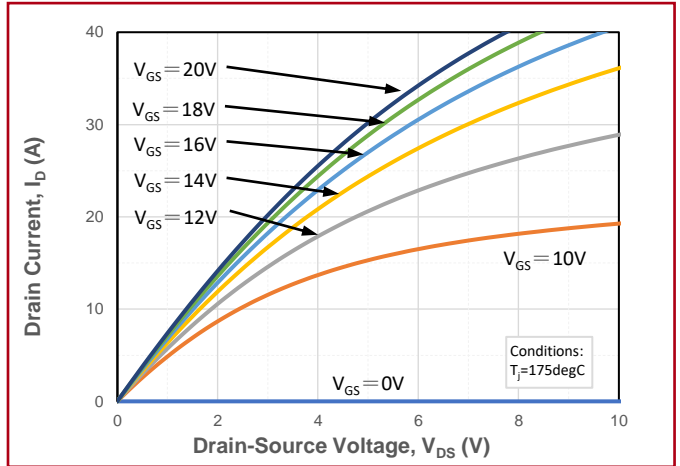


Fig.2 Forward Output Characteristics at $T_j = 175^\circ\text{C}$

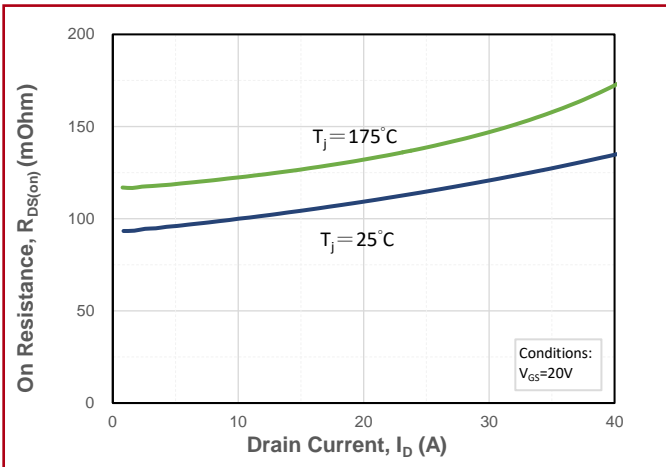


Fig.3 On-Resistance vs. Drain Current for Various T_j

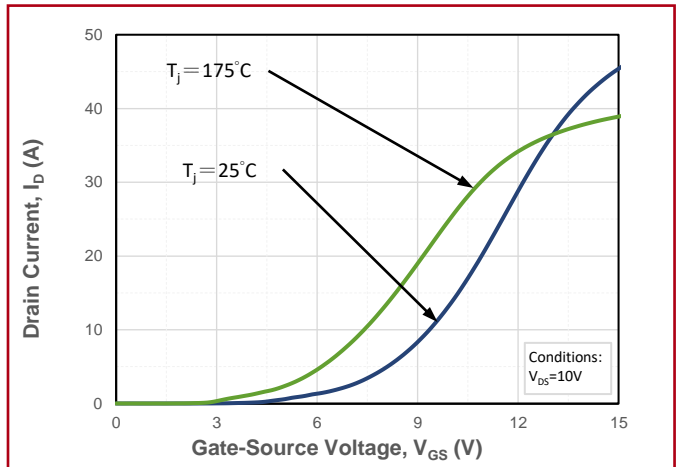


Fig.4 Transfer Characteristics for Various T_j

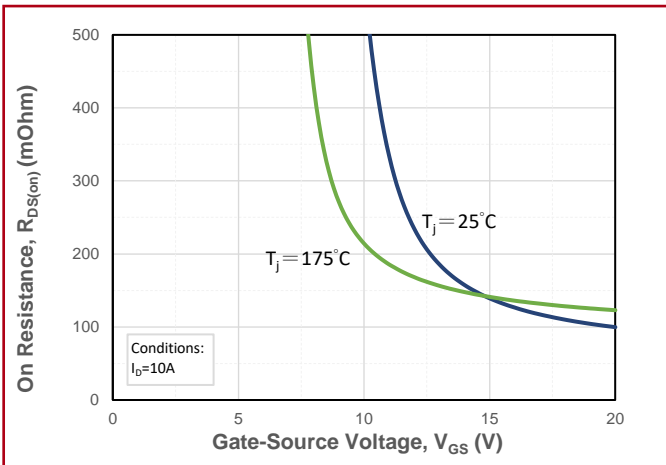


Fig.5 On-Resistance vs. Gate Voltage for Various T_j

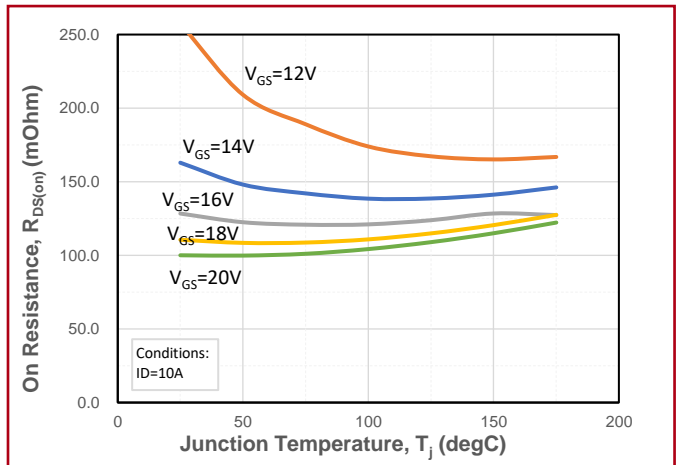


Fig.6 On-Resistance vs. Temperature for Various Gate Voltage

Typical Device Performance

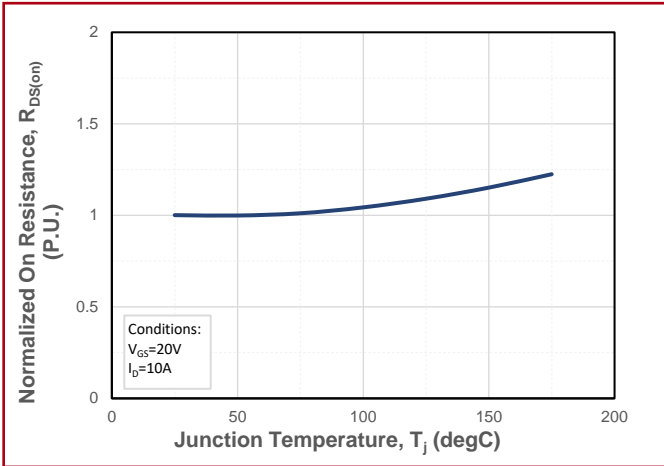


Fig.7 Normalized On-Resistance vs. Temperature

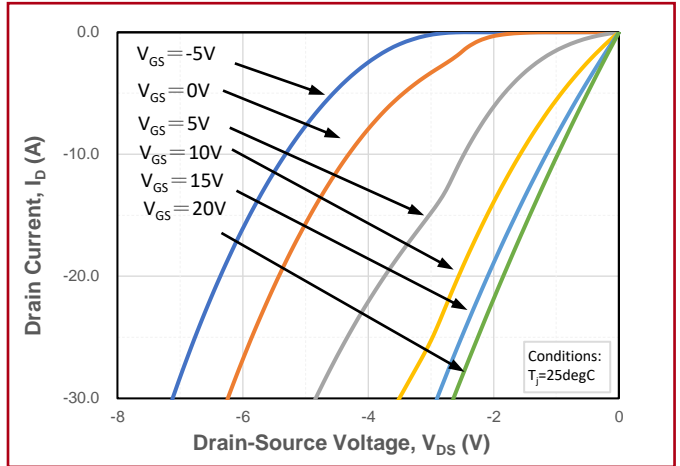


Fig.8 Reverse Output Characteristics at $T_j = 25^\circ C$

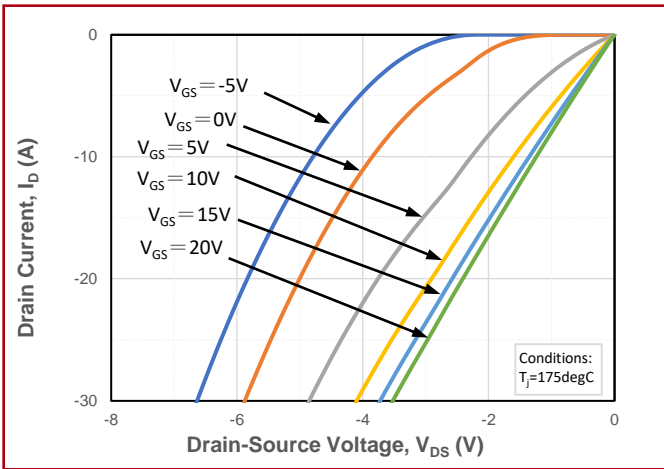


Fig.9 Reverse Output Characteristics at $T_j = 175^\circ C$

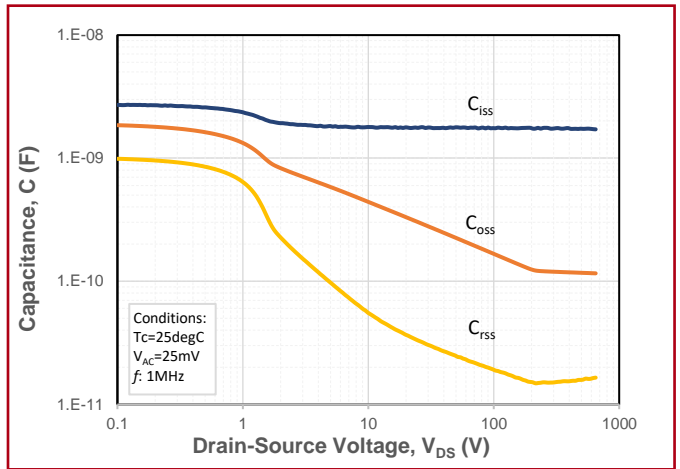


Fig.10 Capacitances vs. Drain to Source Voltage

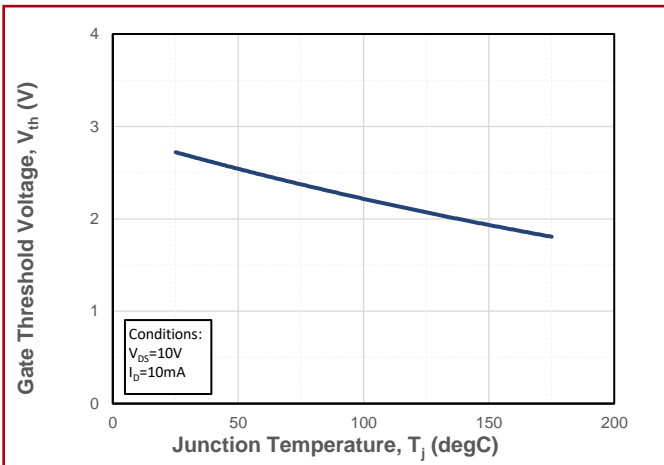


Fig.11 Threshold Voltage vs. Temperature

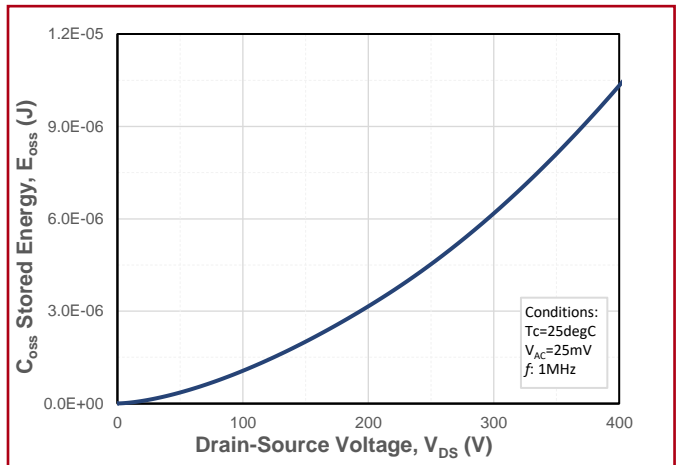


Fig.12 Output Capacitor Stored Energy

Typical Device Performance

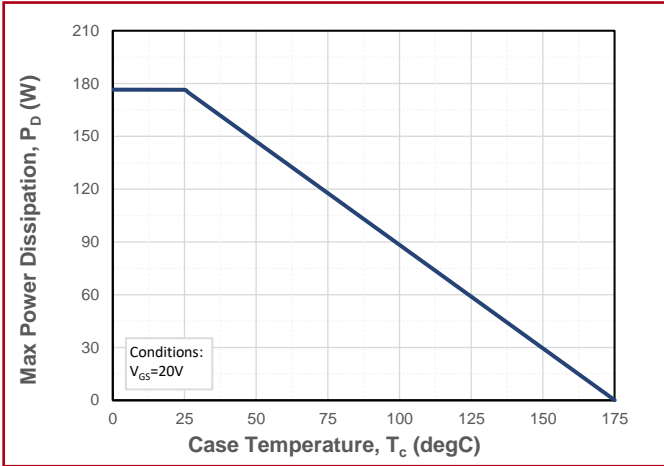


Fig.13 Maximum Power Dissipation Derating vs. Case Temperature

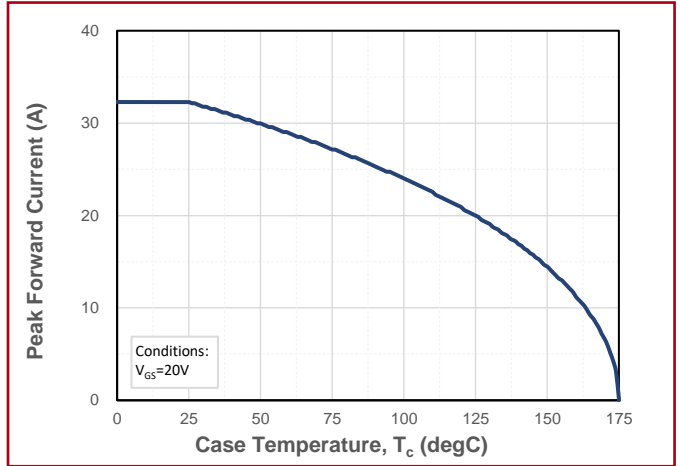


Fig.14 Drain Current Derating vs. Case Temperature

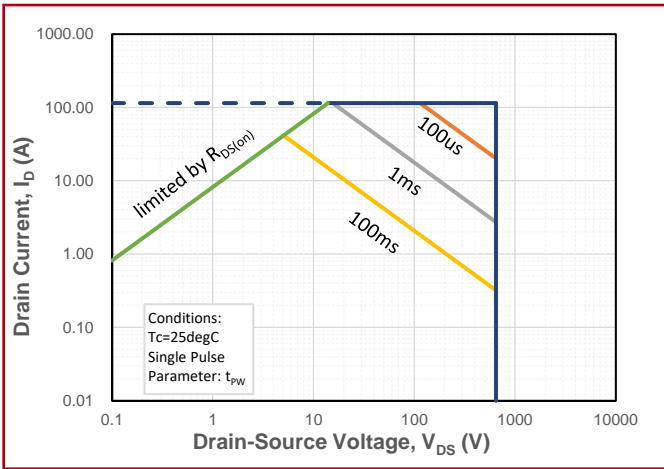


Fig.15 Safe Operating Area

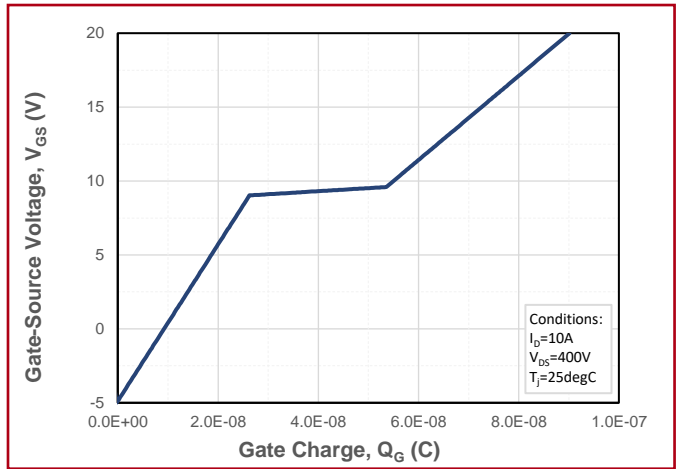


Fig.16 Gate Charge Characteristics

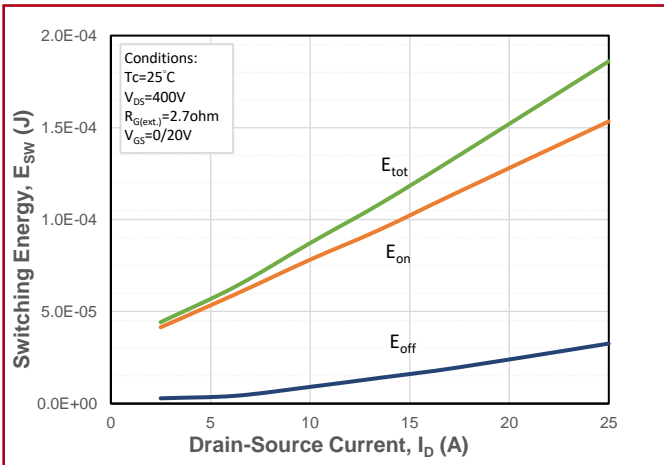


Fig.17 Clamped Inductive Switching Energy vs. Drain Current

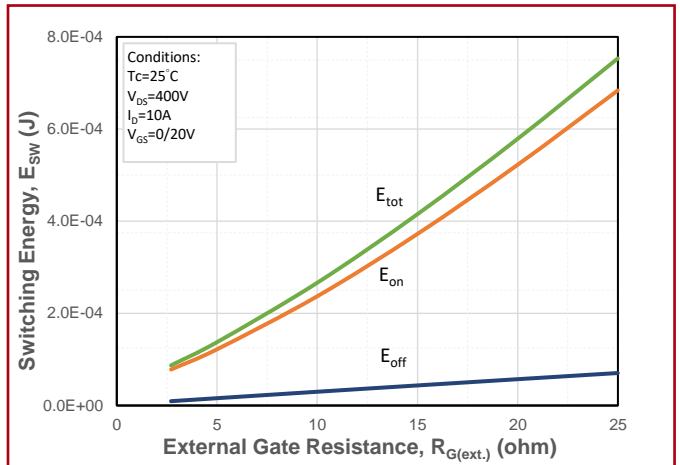


Fig.18 Clamped Inductive Switching Energy vs. External Gate Resistor ($R_{G(ext.)}$)

Typical Device Performance

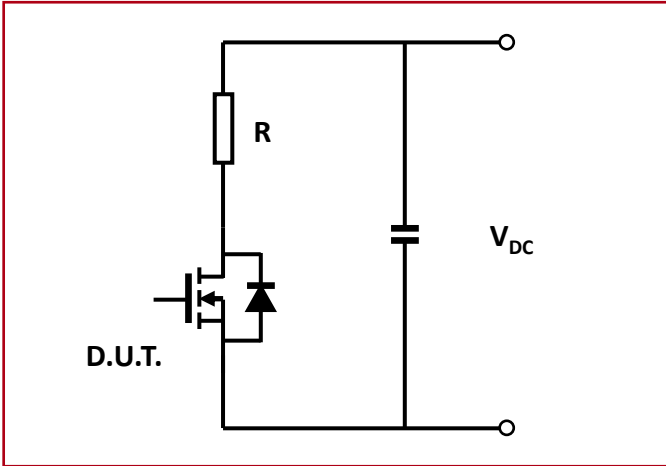


Fig.19 Schematic of Resistive Switching

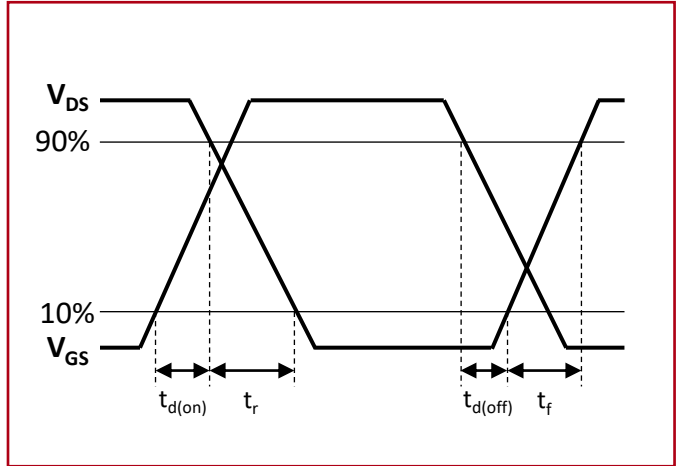


Fig.20 Switching Times Definition

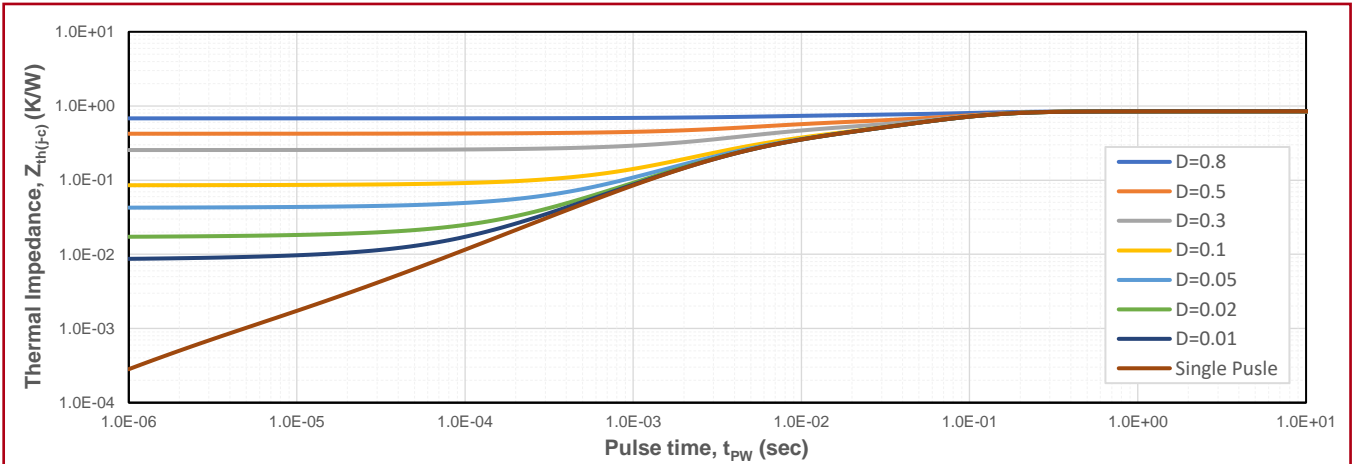


Fig.21 Transient Junction to Case Thermal Impedance

Naming Rule

H2 M 065 B 100

Generation

H2 = 2nd Gen Discrete

Device Type

M = MOSFET J = JMOS

S = JBS diode

Breakdown Voltage

065 = 650V 170 = 1700V

120 = 1200V 330 = 3300V

Package

F = TO-247-3L Q = TO-247-4L

B = TO-220-3L T = TO-263-2L

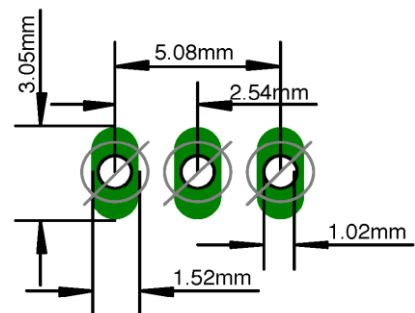
Typical On-Resistance

030 = 30mΩ 040 = 40mΩ 060 = 60mΩ

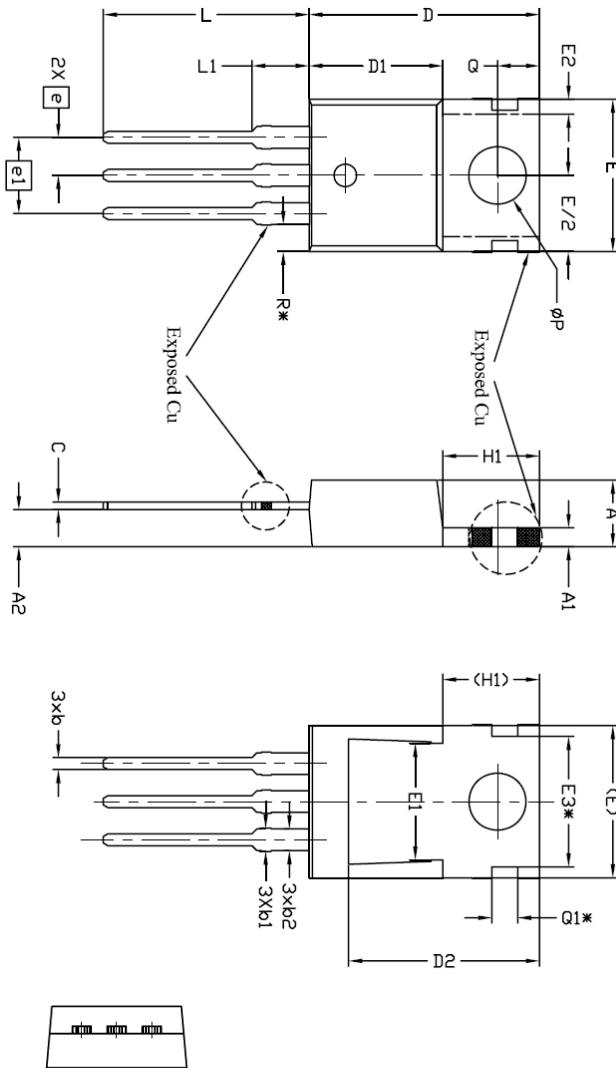
100 = 100mΩ 240 = 240mΩ

Recommended Solder Pad Layout

TO-220-3L



Package Dimensions



Symbol	mm			NOTES
	Min.	Typ.	Max.	
A	4,24	4,44	4,64	
A1	1,15	1,27	1,40	
A2	2,30	2,48	2,70	
b	0,70	0,80	0,90	
b1	1,20	1,55	1,75	
b2	1,20	1,45	1,70	
c	0,40	0,50	0,60	
D	14,70	15,37	16,00	4
D1	8,82	8,92	9,02	
D2	12,43	12,73	12,83	5
E	9,96	10,16	10,36	4,5
E1	6,86	7,77	8,89	5
E2	-	-	0,76	6
E3*	8,70REF.			
e	2,54BSC			
e1	5,08BSC			
H1	6,30	6,45	6,60	5,6
L	13,47	13,72	13,97	
L1	3,60	3,80	4,00	
ϕP	3,75	3,84	3,93	
Q	2,60	2,80	3,00	
Q1*	1,73REF.			
R*	1,82REF.			

Note:

1. Package Reference: JEDEC TO220, Variation AB.
2. All Dimensions Are In mm.
3. Slot Required, Notch May Be Rounded
4. Dimension D & E Do Not Include Mold Flash. Mold Flash Shall Not Exceed 0.127mm Pre Side. These Dimensions Are Measured At The Outermost Extreme Of The Plastic Body.
5. Thermal Pad Contour Optional Within Dimensions E, H1, D2 & E1.
6. Dimension E2 & H1 Define A Zone Where Stamping And Singulation Irregularities Are Allowed.
7. "*" is reference .

Notes

- The information provided herein is subject to change without notice.
- For other information that does not show on this datasheet, please contact us for inquiry.