H1M065B050/T050

Silicon Carbide MOSFET
N-CHANNEL ENHANCEMENT MODE

Product Summary

V_{DS}	650V
$I_{D(@25^{\circ}C)}$	60A
$R_{DS(on)}$	50mΩ

RoHS COMPLIANT
Halogen-Free (F, Cl, I, Br)
AEC-Q101 QUALIFIED

Features

- Low On-Resistance and High Current Density
- Low Capacitance for High Frequency Operation
- Ultra-high Avalanche Ruggedness
- Positive Temperature Coefficient Device
- Low impedance Kelvin source pin-out
- RoHS Compliant and Halogen Free

Benefits

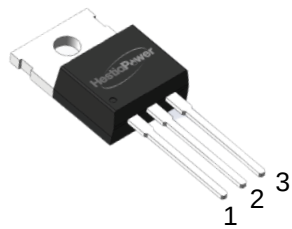
- Higher System Efficiency
- Increase Parallel Device Convenience
- Capable of 175˚C High T_j Application
- Allow High Frequency Operation
- Realize Compact and Lightweight Systems

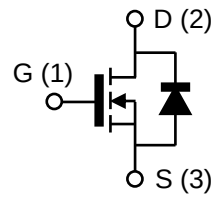
Applications

- Switching Mode Power Supply
- DC/DC Converters, UPS, and PFC
- EV Charging Station
- Motor Drives
- Power Inverters
- Solar/Wind Renewable Energy

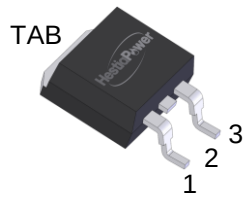
Circuit Diagram

TO-220-3L





TO-263-2L



Part Number	Package	Marking
H1M065B050	TO-220-3L	H1M065B050
H1M065T050	TO-263-2L	H1M065T050

Absolute Maximum Ratings (T_c = 25˚C unless otherwise specified)

Parameter	Symbol	Test Conditions	Value	Unit
Drain – Source Voltage	$V_{DS, max}$	V_{GS}=0V, I_{DS}=100μA	650	V
Continuous Drain Current	I_D	V_{GS}=20V, T_C=25°C	60	A
		V_{GS}=20V, T_C=110°C	41	
Pulse Drain Current	$I_{D, pulse}$	t_{PW} limitation per Fig.15	127	
Avalanche energy, Single Pulse	E_{AS}	V_{DD}=100V, I_D=10A	1600	mJ
Power Dissipation	P_D	T_C=25°C	250	W
Recommend Gate Source Voltage	$V_{GS, op}$	Static, recommended DC operating values	-5 to 20	V
Maximum Gate Source Voltage	$V_{GS, max}$	Transient operating limit (AC f > 1Hz, duty cycle < 1%)	-10 to 25	
Junction & Storage Temperature	T_j, T_{stg}		-55 to 175	°C
Soldering Temperature	T_L		260	
Mounting Torque	M_D	M3 or 6-32 screw	1.0	Nm

Thermal Resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal Resistance, Junction to Case	$R_{\theta,JC}$		0.6		˚C/W

Electrical Characteristics (T_c = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_{DS}=100μA	650			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=10V, I_{DS}=20mA		2.6		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=650V, V_{GS}=0V		<1	50	μA
		V_{DS}=650V, V_{GS}=0V T_j=175°C		10	500	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=20V, V_{DS}=0V			250	nA
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS}=20V, I_{DS}=20A		50	65	mΩ
		V_{GS}=20V, I_{DS}=20A, T_j=175°C		65		
Transconductance	g_{fs}	V_{DS}=15V, I_{DS}=40A		13.2		S
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=400V f =1MHz, V_{AC}=25mV		1850		pF
Output Capacitance	C_{oss}			208		
Reverse Transfer Capacitance	C_{rss}			33		
Effective Output Capacitance, Energy Related	$C_{o(er)}$	V_{GS}=0V, V_{DS}=0 to 400V		237		
Effective Output Capacitance, Time Related	$C_{o(tr)}$	I_D=const., V_{GS}=0V, V_{DS}=0 to 400V		305		
Short-Circuit Withstand Time	t_{SC}	V_{GS}=0/15V, V_{DS}=400V R_G=100Ω		<18		μs
Turn On Delay Time	$t_{d(on)}$	V_{DS}=400V, V_{GS}=-4/+20V, I_D=20A, R_L=20Ω, $R_{G(ext)}$= 2.7 Ω		16		ns
Rise Time	t_r			17		
Turn Off Delay Time	$t_{d(off)}$			20		
Fall Time	t_f			10		
C_{oss} Stored Energy	E_{oss}	V_{GS}=0V, V_{DS}=400V f =1MHz, V_{AC}=25mV		24		μJ
Turn-on Switching Energy	E_{on}	V_{DS}=400V, V_{GS}=0/20V, I_D=12A, $R_{G(ext)}$= 2.7 Ω		85.9		
Turn-off Switching Energy	E_{off}			20.1		
Internal Gate Resistance	$R_{G(int.)}$	f =1MHz, V_{AC}=25mV		1.2		Ω

Built-in SiC Diode Characteristics (T_c = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Typ.	Unit
Inverse Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_{SD}=5A	3.0	V
Continuous Diode Forward Current	I_S	V_{GS}=0V, T_C=25°C	42.5	A
Reverse Recovery Time	t_{rr}	V_{GS}=0V, I_{SD}=30A, V_{DS}=400V, di/dt=300A/μs	58	ns
Reverse Recovery Charge	Q_{rr}		122	nC
Peak Reverse Recovery Current	I_{rrm}		3.75	A

Gate Charge Characteristics (T_c = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Value	Unit
Gate to Source Charge	Q_{GS}	V_{DS}=400V, V_{GS}=-5/+20V, I_D=30A	30	nC
Gate to Drain Charge	Q_{GD}		43	
Total Gate Charge	Q_G		121	
Gate plateau voltage	V_{pl}		8.8	V

Typical Device Performance

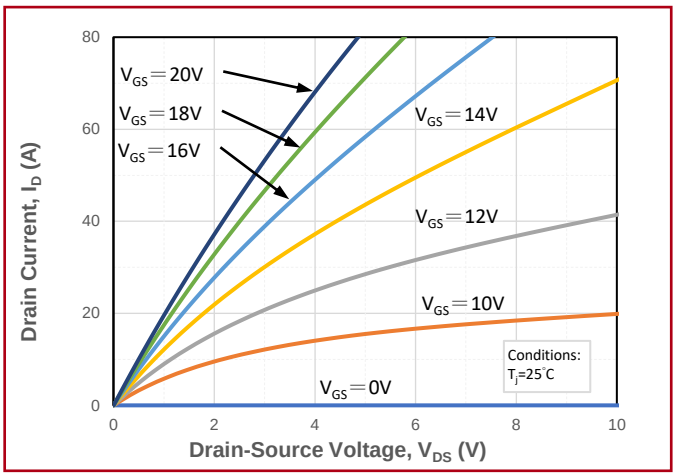


Fig.1 Forward Output Characteristics at T_j=25˚C

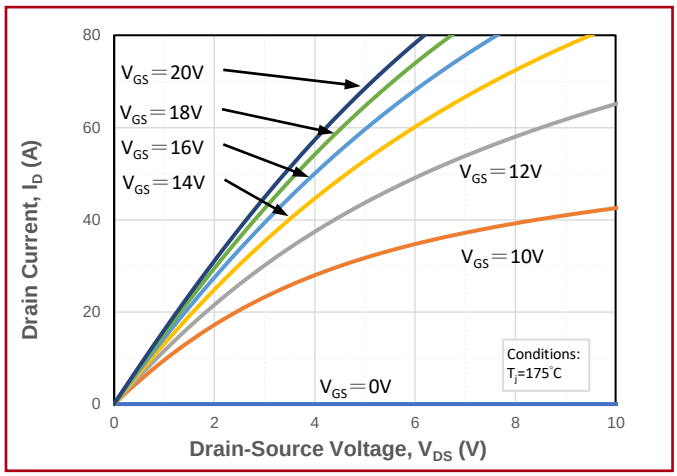


Fig.2 Forward Output Characteristics at T_j=175˚C

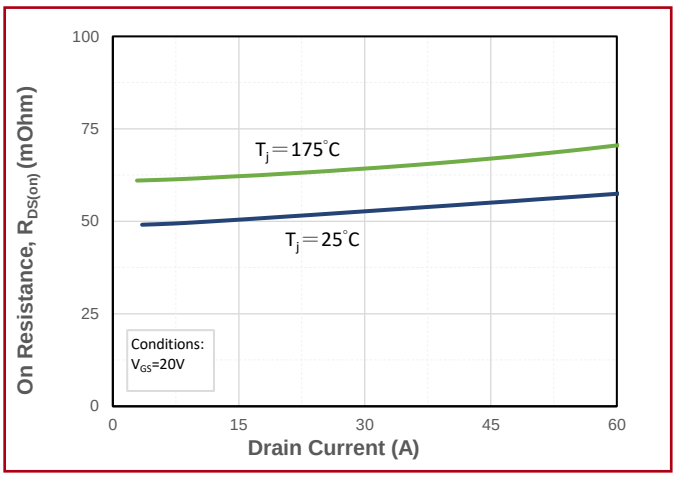


Fig.3 On-Resistance vs. Drain Current for Various T_j

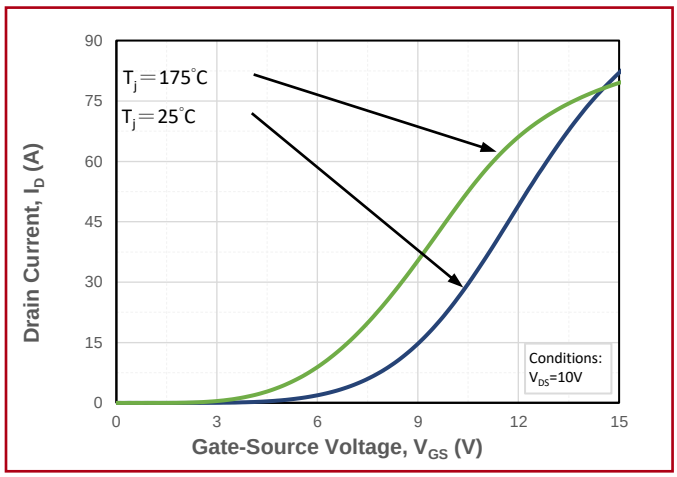


Fig.4 Transfer Characteristics for Various T_j

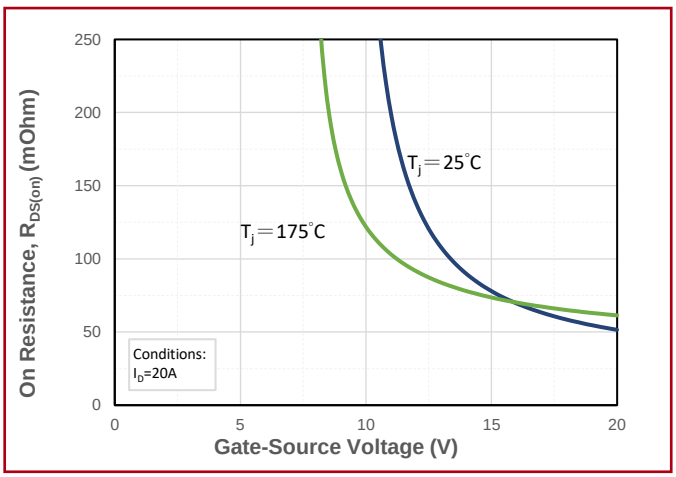


Fig.5 On-Resistance vs. Gate Voltage for Various T_j

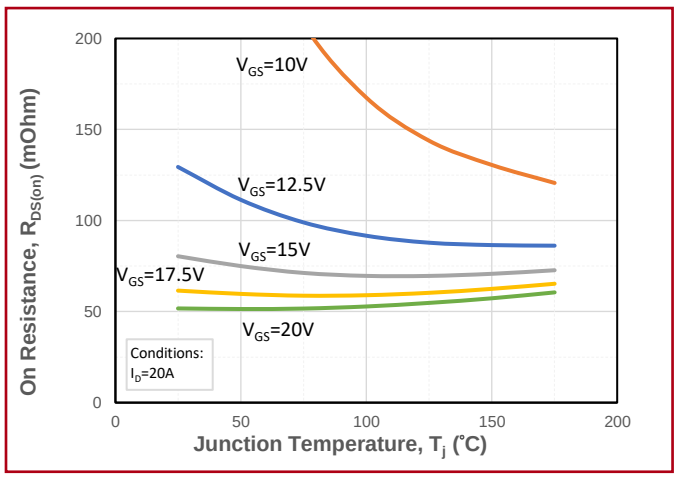


Fig.6 On-Resistance vs. Temperature for Various Gate Voltage

Typical Device Performance

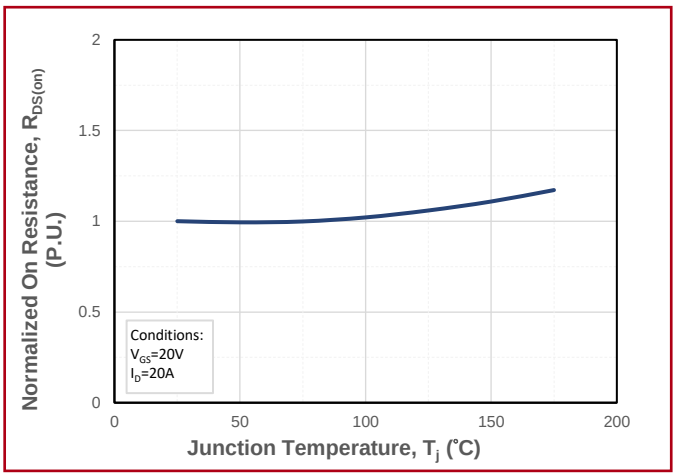


Fig.7 Normalized On-Resistance vs. Temperature

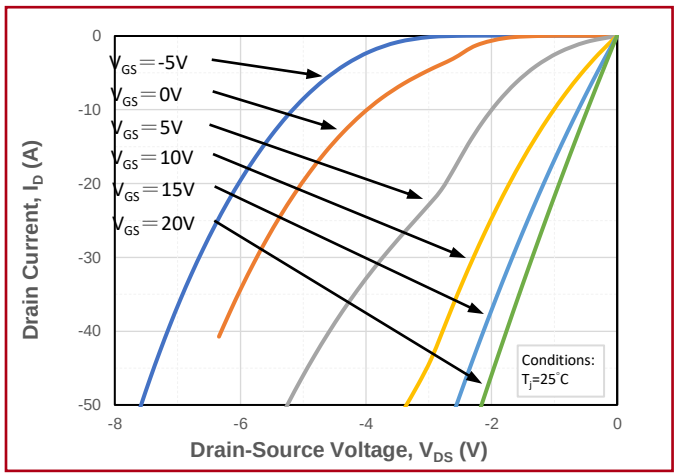


Fig.8 Reverse Output Characteristics at T_j = 25°C

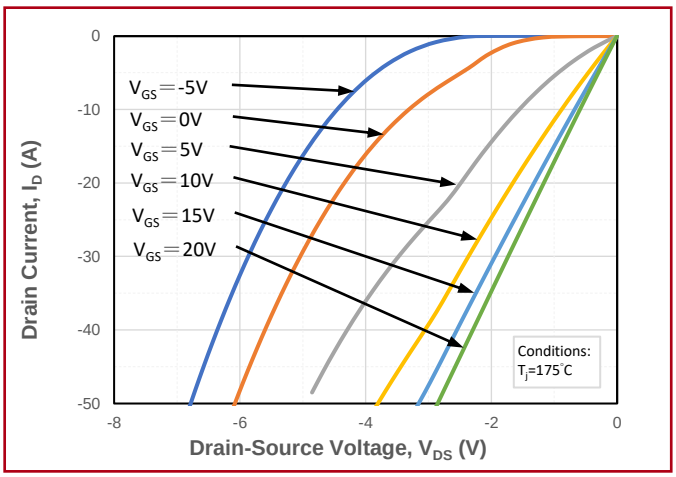


Fig.9 Reverse Output Characteristics at T_j = 175°C

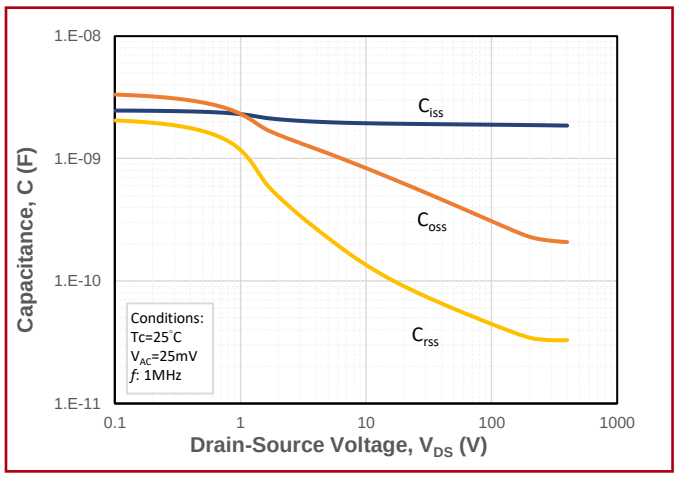


Fig.10 Capacitances vs. Drain to Source Voltage

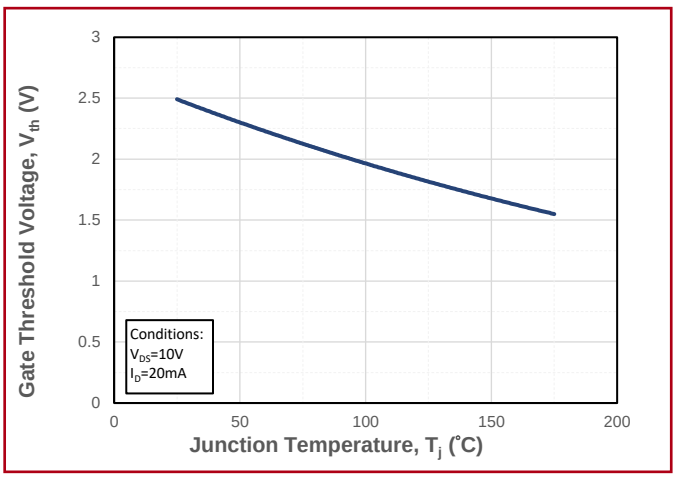


Fig.11 Threshold Voltage vs. Temperature

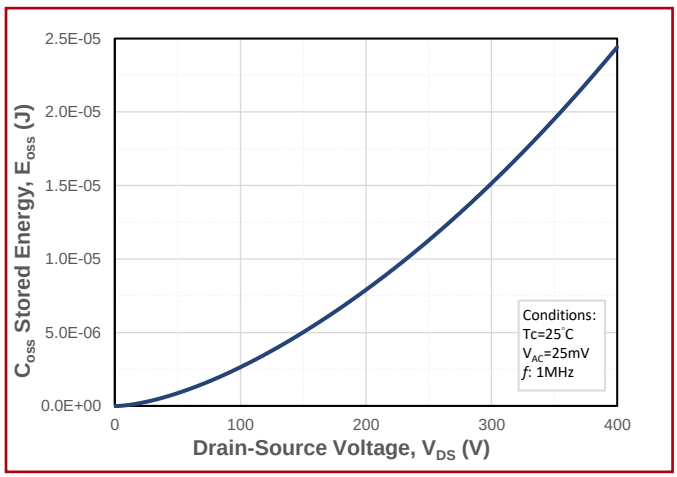


Fig.12 Output Capacitor Stored Energy

Typical Device Performance

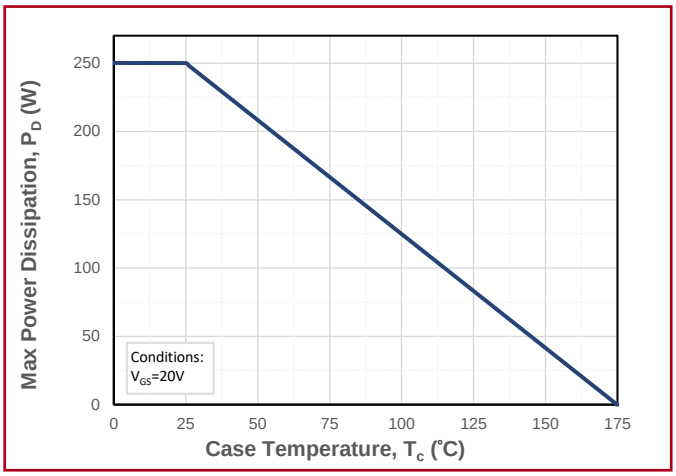


Fig.13 Maximum Power Dissipation Derating vs. Case Temperature

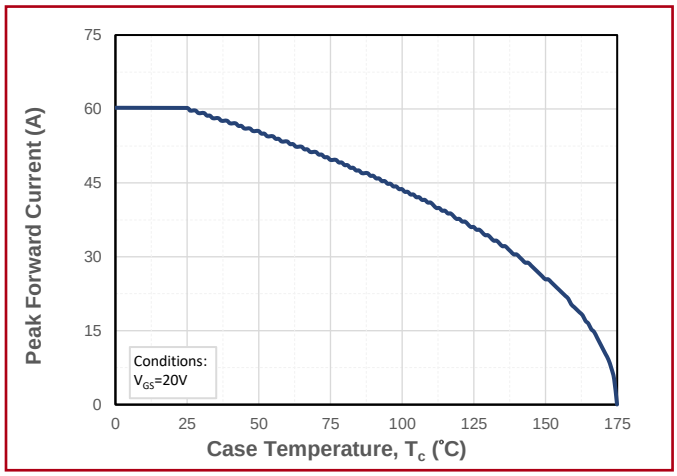


Fig.14 Drain Current Derating vs. Case Temperature

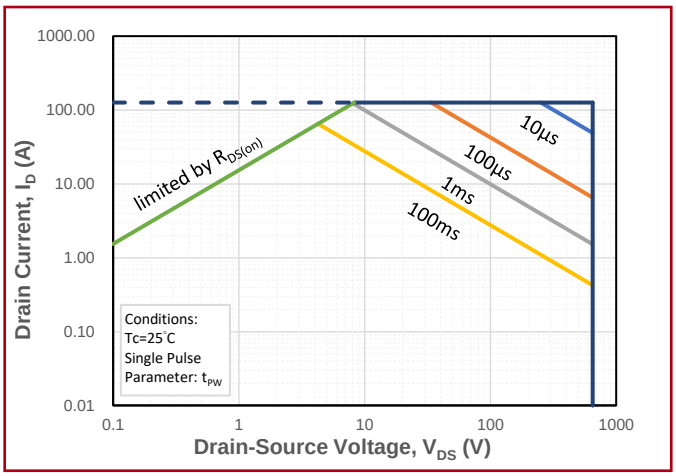


Fig.15 Safe Operating Area

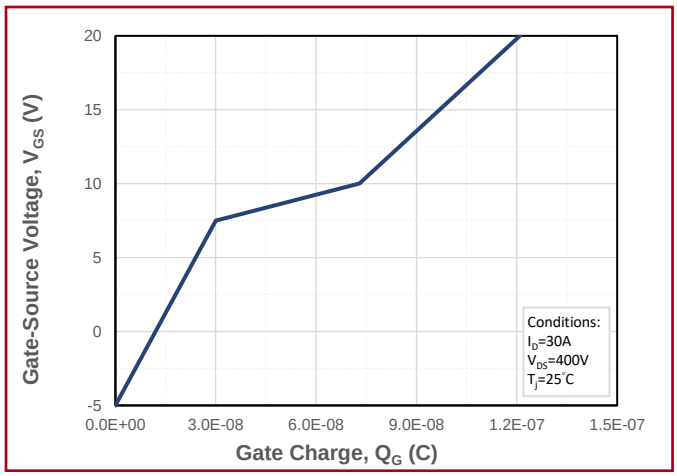


Fig.16 Gate Charge Characteristics

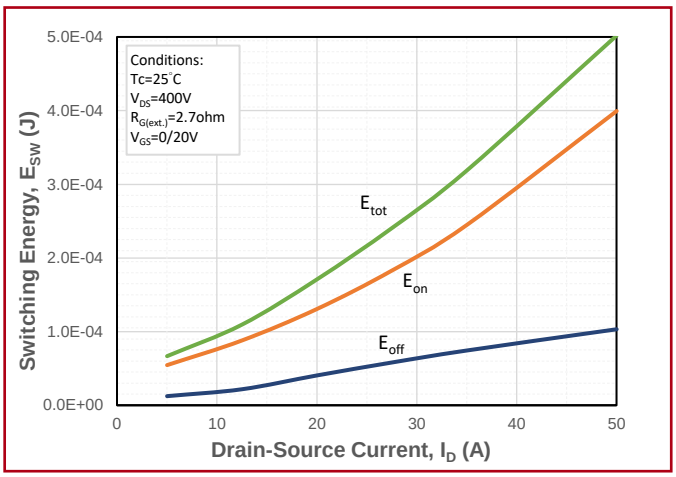


Fig.17 Clamped Inductive Switching Energy vs. Drain Current

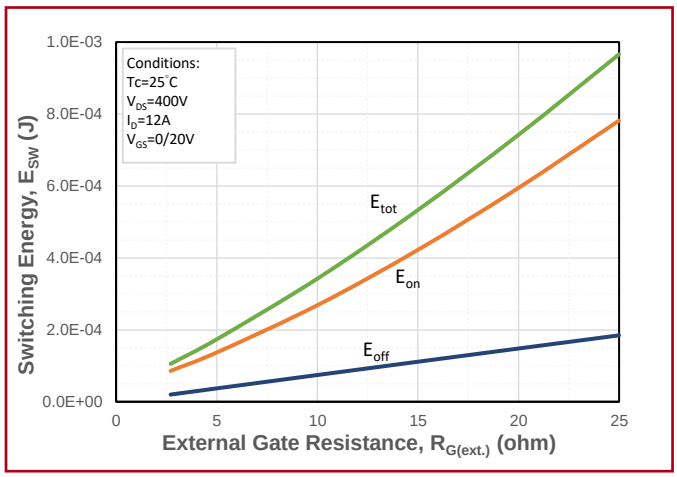


Fig.18 Clamped Inductive Switching Energy vs. External Gate Resistor ($R_{G(ext.)}$)

Typical Device Performance

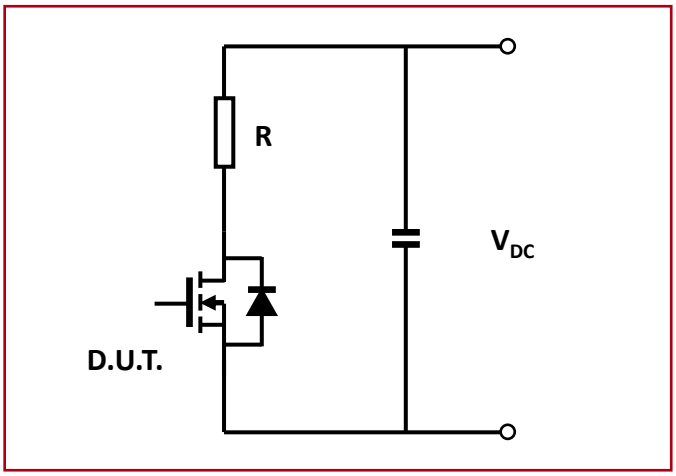


Fig.19 Schematic of Resistive Switching

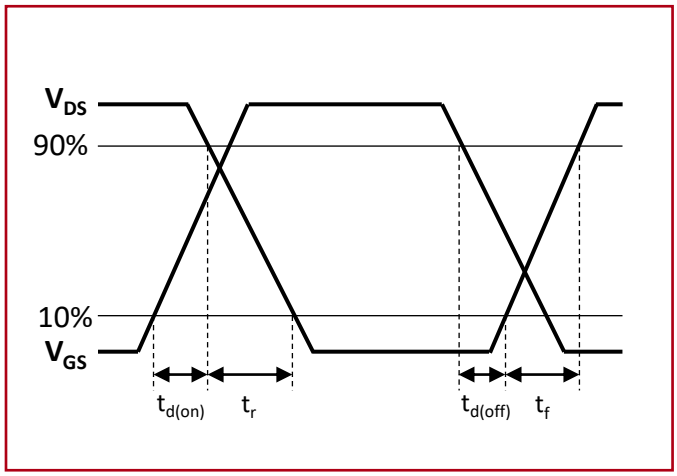


Fig.20 Switching Times Definition

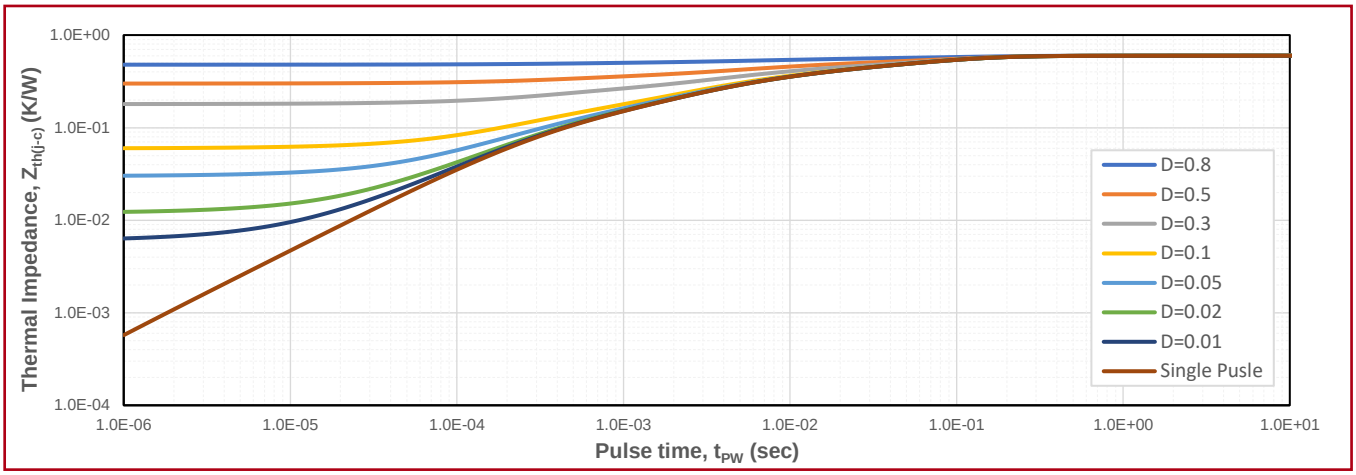


Fig.21 Transient Junction to Case Thermal Impedance

Naming Rule

H1 M 065 B 050

Generation
H1 = Gen 1st Discrete

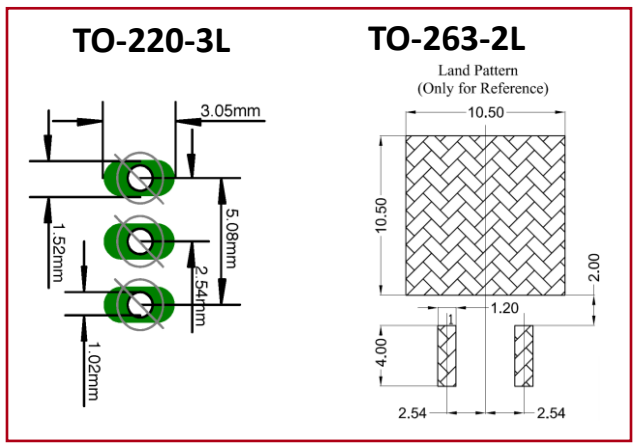
Device Type
M = MOSFET J = JMOS
S = JBS diode

Breakdown Voltage
065 = 650V 170 = 1700V
120 = 1200V 330 = 3300V

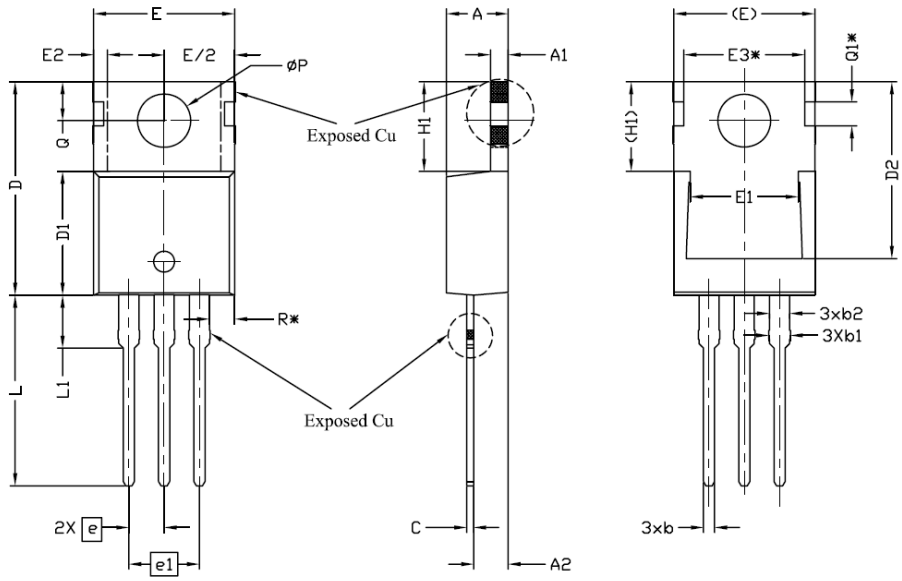
Package
Q = TO-220-2L, TO-263-2L B = TO-220-3L
T = TO-263-2L N = Bare Die

Typical On-Resistance
020 = 20mΩ 050 = 50mΩ 100 = 100mΩ
200 = 200mΩ

Recommended Solder Pad Layout



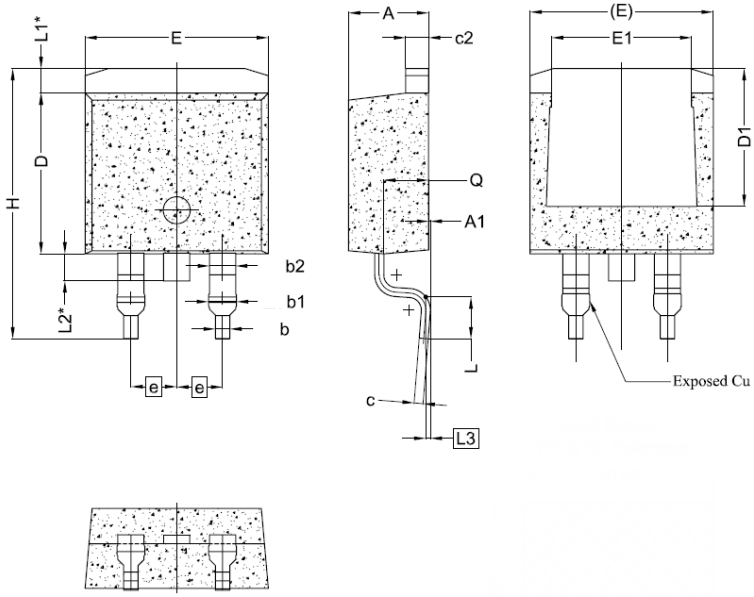
Package Dimensions (TO-220-3L)



Note:
1. Package Reference: JEDEC TO220, Variation AB.
2. All Dimensions Are In mm.
3. Slot Required, Notch May Be Rounded
4. Dimension D & E Do Not Include Mold Flash. Mold Flash Shall Not Exceed 0.127mm Pre Side. These Dimensions Are Measured At The Outermost Extreme Of The Plastic Body.
5. Thermal Pad Contour Optional Within Dimensions E, H1, D2 & E1.
6. Dimension E2 & H1 Define A Zone Where Stamping And Singulation Irregularities Are Allowed.
7. "*" is reference .

Symbol	mm			NOTES
	Min.	Typ.	Max.	
A	4,24	4,44	4,64	
A1	1.15	1.27	1.40	
A2	2.30	2.48	2.70	
b	0.70	0.80	0.90	
b1	1,20	1.55	1.75	
b2	1,20	1.45	1.70	
c	0.40	0.50	0.60	
D	14.70	15.37	16.00	4
D1	8,82	8,92	9,02	
D2	12.43	12.73	12.83	5
E	9.96	10.16	10.36	4,5
E1	6,86	7,77	8,89	5
E2	-	-	0,76	6
E3*	8,70REF.			
e	2.54BSC			
e1	5,08BSC			
H1	6,30	6,45	6,60	5,6
L	13.47	13.72	13.97	
L1	3.60	3.80	4.00	
ØP	3,75	3,84	3,93	
Q	2,60	2,80	3,00	
Q1*	1,73REF.			
R*	1,82REF.			

Package Dimensions (TO-263-2L, TO-263-2L-1NC)



Note:
1. All Dimensions Are In mm.
2. Dimension D & E Do Not Include Mold Flash. Mold Flash Shall Not Exceed 0.127mm Pre Side. These Dimensions Are Measured At The Outermost Extreme Of The Plastic Body.
3. Thermal Pad Contour Optional Within Dimensions E, L1, D1 & E1.
4. Dimension D1 & E1 Establish A Minmum Mounting Surface for The Thermal Pad.
5. "*" is reference .

Symbol	mm		
	Min.	Typ.	Max.
A	4.24	4.44	4.64
A1	0.00	0.10	0.25
b	0.70	0.80	0.90
b1	1.20	1.55	1.75
b2	1.20	1.45	1.70
c	0.40	0.50	0.60
c2	1.15	1.27	1.40
D	8.82	8.92	9.02
D1	6.86	7.65	---
E	9.96	10.16	10.36
E1	6.89	7.77	7.89
e	2.54 BSC		
e1	5.08 BSC		
H	14.61	15.00	15.88
L	1.78	2.32	2.79
L1	1.36 REF		
L2	0.00 REF (TO-263-2L) 1.50 REF (TO-263-2L-1NC)		
L3	0.25 BSC		
Q	2.30	2.48	2.70