H2M120Q040

Silicon Carbide MOSFET
N-CHANNEL ENHANCEMENT MODE

Features

- Low On-Resistance and High Current Density
- Low Capacitance for High Frequency Operation
- Ultra-high Avalanche Ruggedness
- Positive Temperature Coefficient Device
- Low impedance Kelvin source pin-out
- RoHS Compliant and Halogen Free

Benefits

- Higher System Efficiency
- Increase Parallel Device Convenience
- Capable of 175˚C High T_j Application
- Allow High Frequency Operation
- Realize Compact and Lightweight Systems

Applications

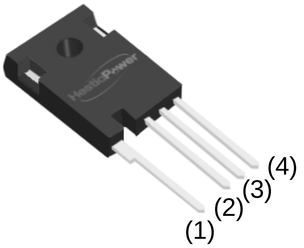
- Switching Mode Power Supply
- DC/DC Converters, UPS, and PFC
- EV Charging Station
- Motor Drives
- Power Inverters
- Solar/Wind Renewable Energy

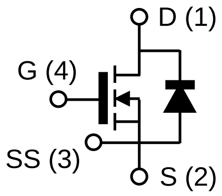
Product Summary

V_{DS}	1200V
$I_{D(@25˚C)}$	65A
$R_{DS(on)}$	40mΩ

RoHS COMPLIANT
Halogen-Free F Cl I Br
AEC-Q101 QUALIFIED

Circuit Diagram





Part Number	Package	Marking
H2M120Q040	TO-247-4L	H2M120Q040

Description

The H2M120Q040 1200V, 40mΩ silicon carbide power MOSFET is an N-channel enhancement mode device. Exploiting the outstanding wide bandgap material properties, this device shows high current density and great switching behavior. Thanks for the excellent thermal conductivity and many advantages of SiC, this device significantly improved in thermal capability and temperature independent switching behavior.

Absolute Maximum Ratings (T_c = 25˚C unless otherwise specified)

Parameter	Symbol	Test Conditions	Value	Unit
Drain – Source Voltage	$V_{DS,\ max}$	V_{GS}=0V, I_{DS}=100µA	1200	V
Continuous Drain Current	I_D	V_{GS}=20V, T_C=25°C	65	A
		V_{GS}=20V, T_C=100°C	48	
Pulse Drain Current	$I_{D,\ pulse}$	t_{PW} limitation per Fig.15	237	
Power Dissipation	P_D	T_C=25°C	341	W
Recommend Gate Source Voltage	$V_{GS,\ op}$	Static, recommended DC operating values	-5 to 20	V
Maximum Gate Source Voltage	$V_{GS,\ max}$	Transient operating limit (AC f > 1Hz, duty cycle < 1%)	-10 to 25	
Junction & Storage Temperature	T_j , T_{stg}		-55 to 175	°C
Soldering Temperature	T_L		260	
Mounting Torque	M_D	M3 or 6-32 screw	1.0	Nm

Thermal Resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal Resistance, Junction to Case	$R_{\theta,JC}$		0.44		˚C/W

Electrical Characteristics (T_c = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_{DS}=100µA	1200			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=10V, I_{DS}=40mA	1.5	2.9	4.5	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=1200V, V_{GS}=0V		<1	50	µA
		V_{DS}=1200V, V_{GS}=0V T_j=175°C		10		
Gate-Source Leakage Current	I_{GSS}	V_{GS}=20V, V_{DS}=0V			250	nA
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS}=20V, I_{DS}=30A		40	50	mΩ
		V_{GS}=20V, I_{DS}=30A, T_j=175°C		69		
Transconductance	g_{fs}	V_{DS}=9.7V, I_{DS}=30A		13		S
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=800V f =1MHz, V_{AC}=25mV		5757		pF
Output Capacitance	C_{oss}			156		
Reverse Transfer Capacitance	C_{rss}			9		
Effective Output Capacitance, Energy Related	$C_{o(er)}$	V_{GS}=0V, V_{DS}=0 to 800V		202		
Effective Output Capacitance, Time Related	$C_{o(tr)}$	I_D=const., V_{GS}=0V, V_{DS}=0 to 800V		284		
Turn On Delay Time	$t_{d(on)}$	V_{DS}=800V, V_{GS}=-5/+20V, I_D=30A, R_L=27Ω, $R_{G(ext)}$= 2.7 Ω		35.2		ns
Rise Time	t_r			56		
Turn Off Delay Time	$t_{d(off)}$			48		
Fall Time	t_f			44.8		
C_{oss} Stored Energy	E_{oss}	V_{GS}=0V, V_{DS}=800V f =1MHz, V_{AC}=25mV		63		µJ
Turn-on Switching Energy	E_{on}	V_{DS}=800V, V_{GS}=0/+20V, I_D=30A, $R_{G(ext)}$= 2.7 Ω		224		
Turn-off Switching Energy	E_{off}			57.4		
Internal Gate Resistance	$R_{G(int.)}$	f =1MHz, V_{AC}=25mV		0.5		Ω

Built-in SiC Diode Characteristics (T_c = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Typ.	Unit
Inverse Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_{SD}=7.5A	2.5	V
Continuous Diode Forward Current	I_S	V_{GS}=0V, T_C=25°C	83	A
Reverse Recovery Time	t_{rr}	V_{GS}=0V, I_{SD}=30A, V_{DS}=400V, di/dt=300A/µs	61	ns
Reverse Recovery Charge	Q_{rr}		155	nC
Peak Reverse Recovery Current	I_{rrm}		4.8	A

Gate Charge Characteristics (T_c = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Value	Unit
Gate to Source Charge	Q_{GS}	V_{DS}=800V, V_{GS}=-5/+20V, I_D=30A	98	nC
Gate to Drain Charge	Q_{GD}		84	
Total Gate Charge	Q_G		298	
Gate plateau voltage	V_{pl}		8.9	V

Typical Device Performance

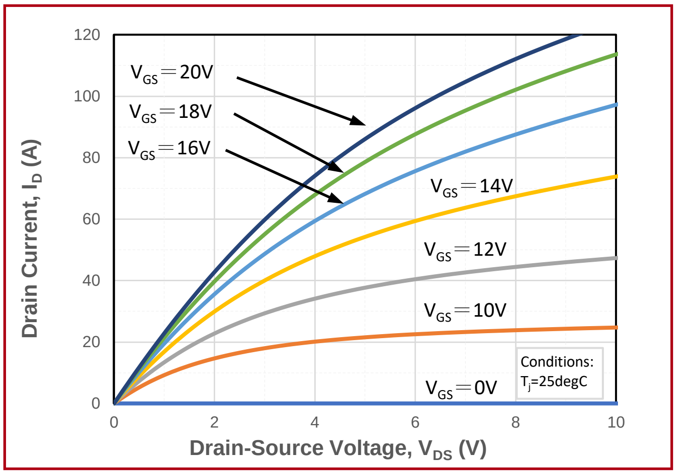


Fig.1 **Forward Output Characteristics at T_j=25˚C**

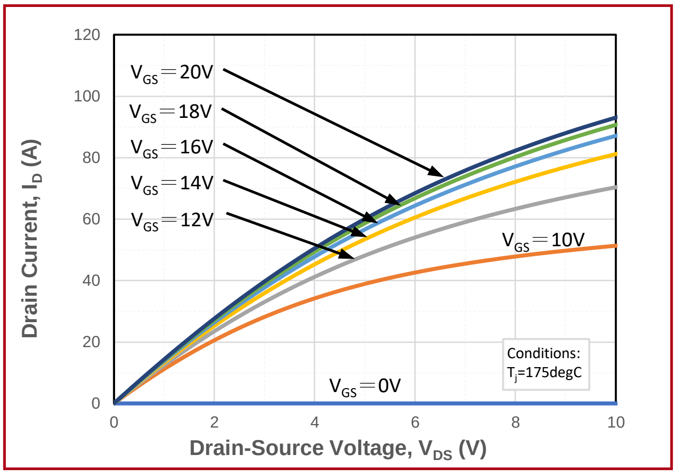


Fig.2 **Forward Output Characteristics at T_j=175˚C**

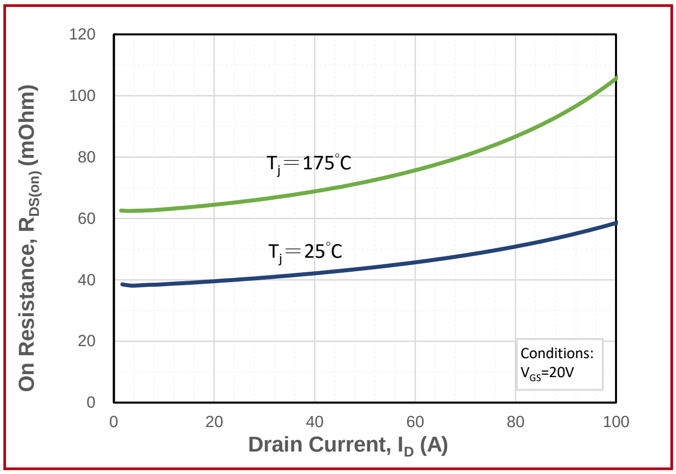


Fig.3 **On-Resistance vs. Drain Current for Various T_j**

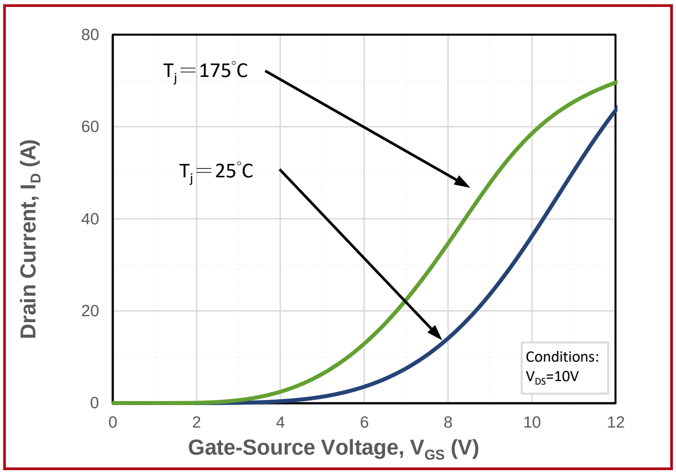


Fig.4 **Transfer Characteristics for Various T_j**

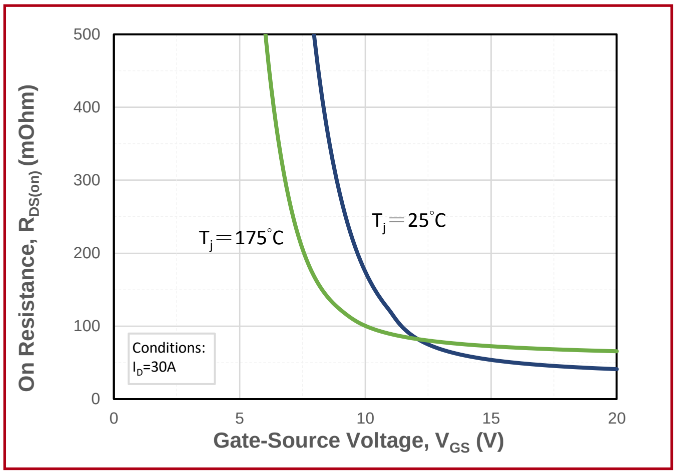


Fig.5 **On-Resistance vs. Gate Voltage for Various T_j**

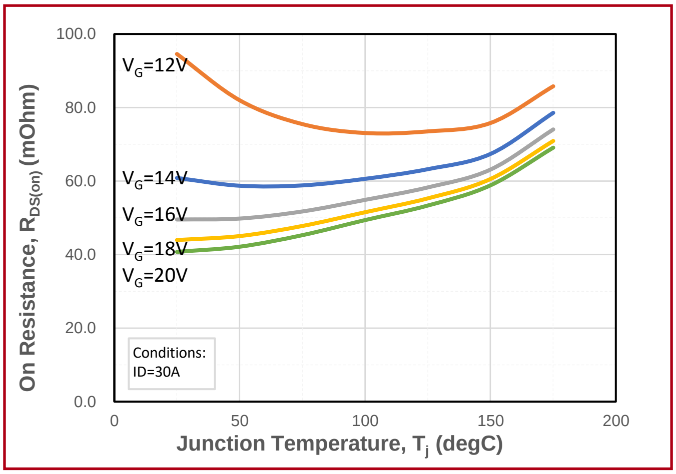


Fig.6 **On-Resistance vs. Temperature for Various Gate Voltage**

Typical Device Performance

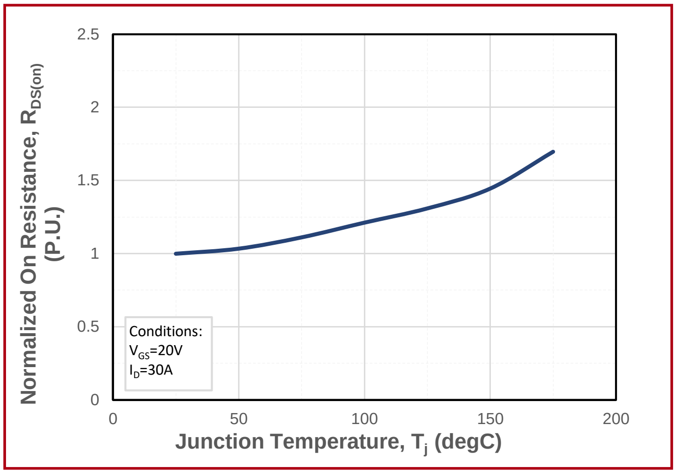


Fig.7 Normalized On-Resistance vs. Temperature

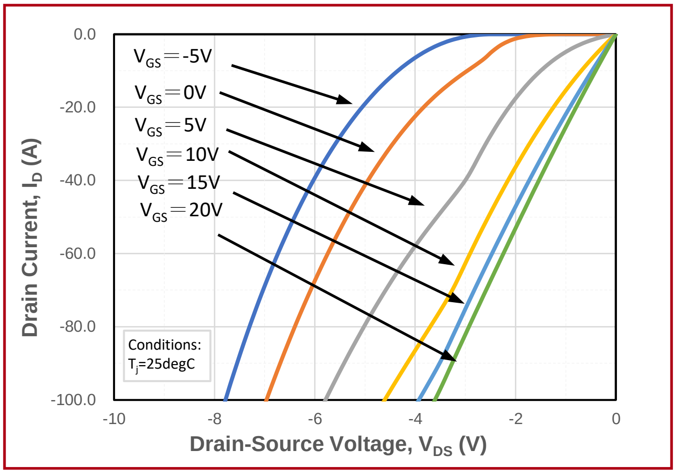


Fig.8 Reverse Output Characteristics at T_j = 25˚C

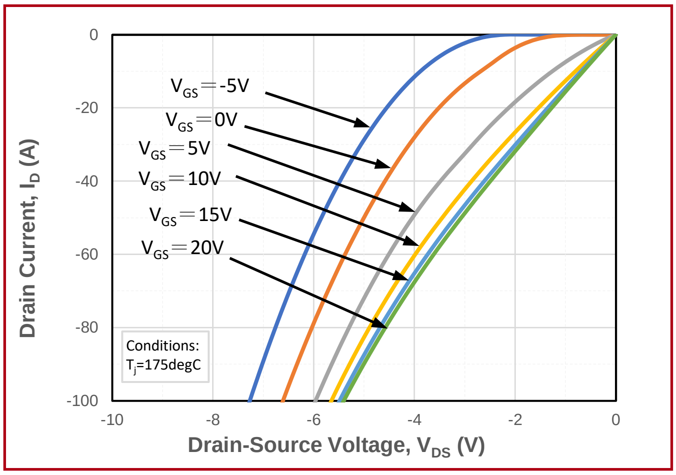


Fig.9 Reverse Output Characteristics at T_j = 175˚C

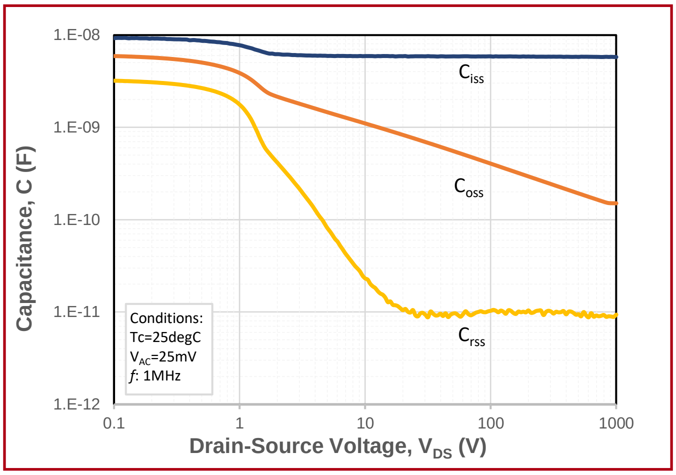


Fig.10 Capacitances vs. Drain to Source Voltage

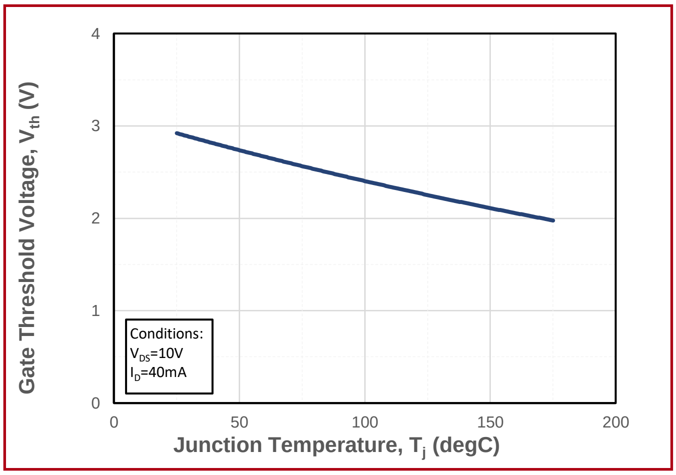


Fig.11 Threshold Voltage vs. Temperature

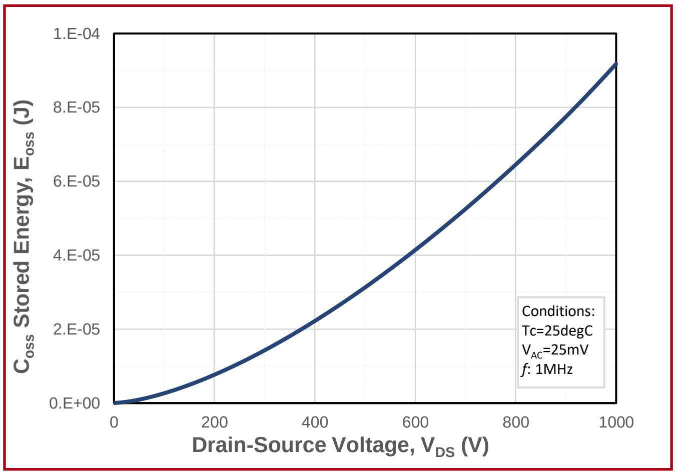


Fig.12 Output Capacitor Stored Energy

Typical Device Performance

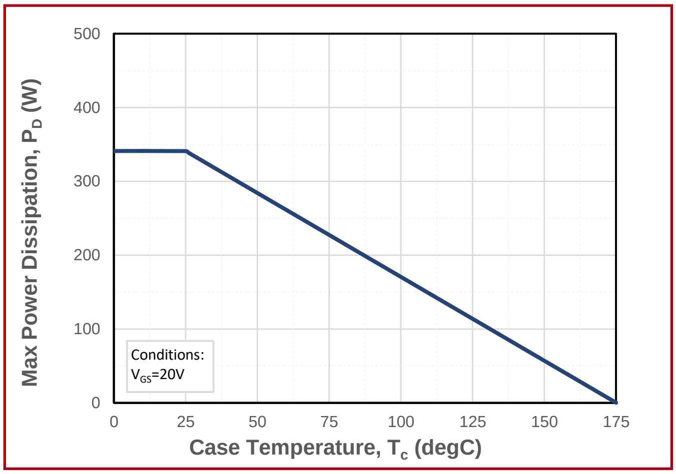


Fig.13 Maximum Power Dissipation Derating vs. Case Temperature

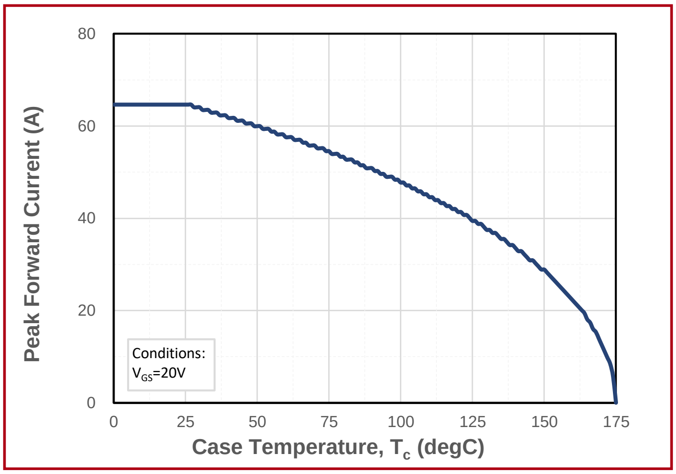


Fig.14 Drain Current Derating vs. Case Temperature

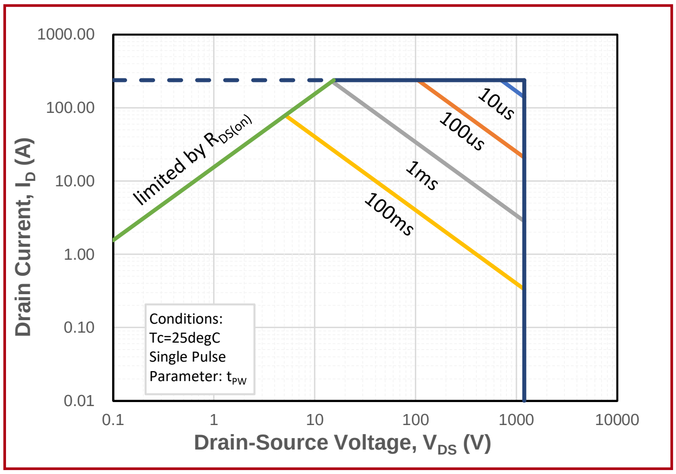


Fig.15 Safe Operating Area

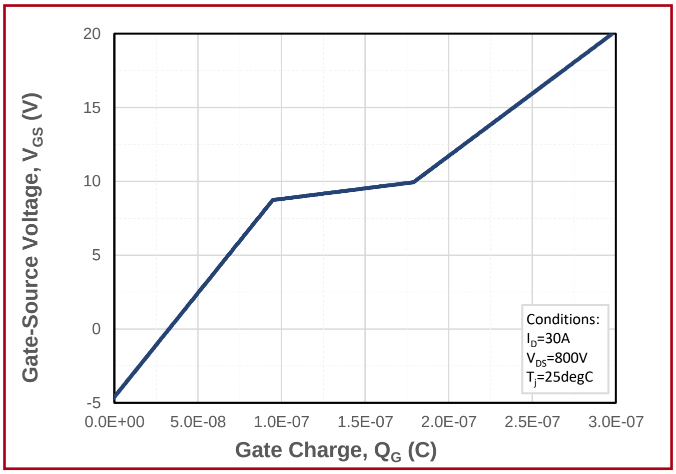


Fig.16 Gate Charge Characteristics

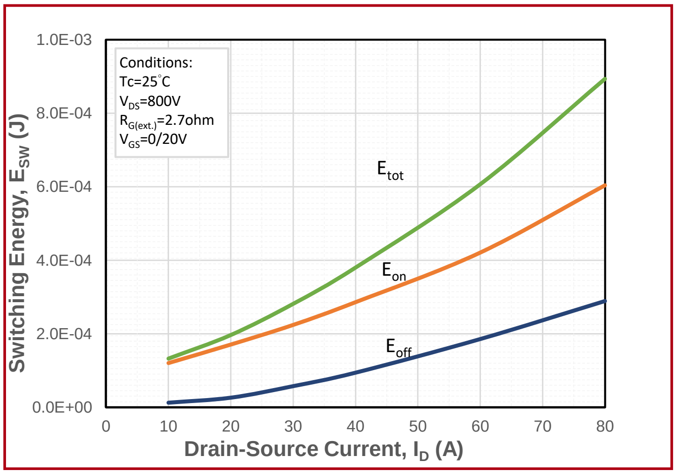


Fig.17 Clamped Inductive Switching Energy vs. Drain Current

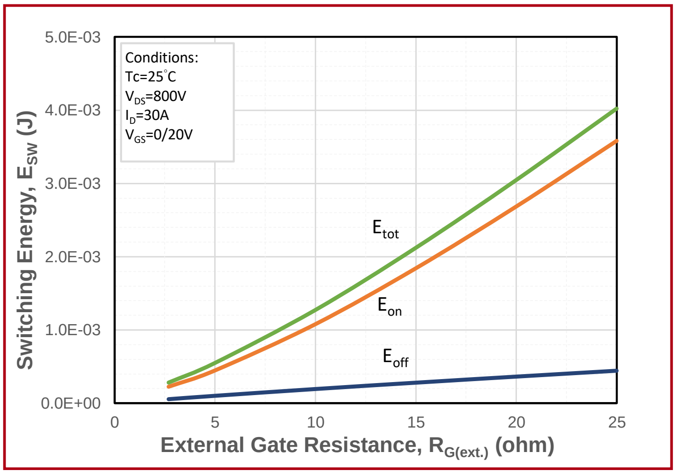
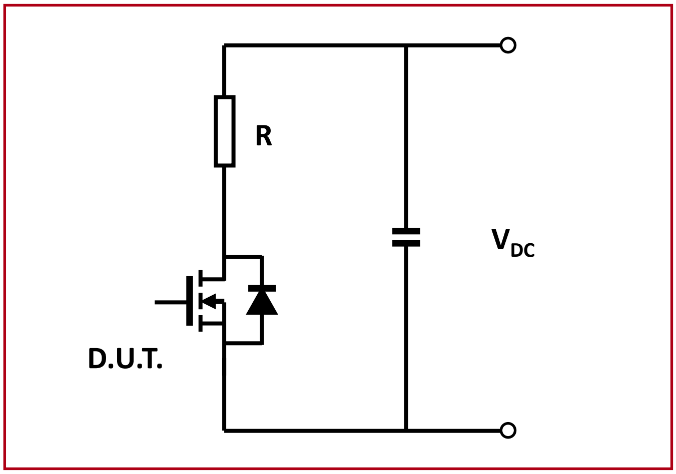


Fig.18 Clamped Inductive Switching Energy vs. External Gate Resistor ($R_{G(ext.)}$)

Typical Device Performance



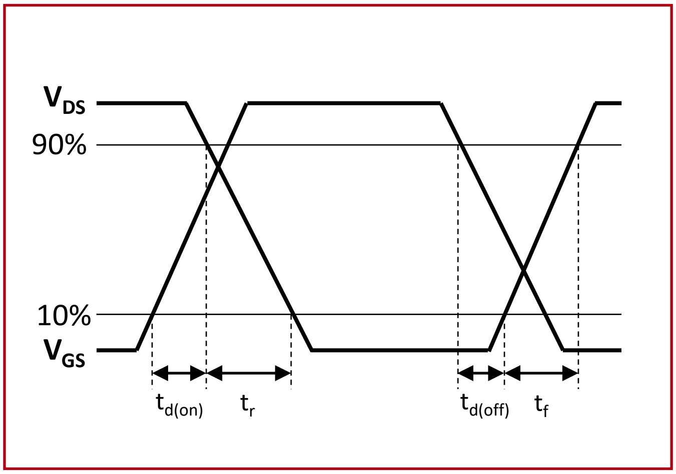


Fig.19 Schematic of Resistive Switching

Fig.20 Switching Times Definition

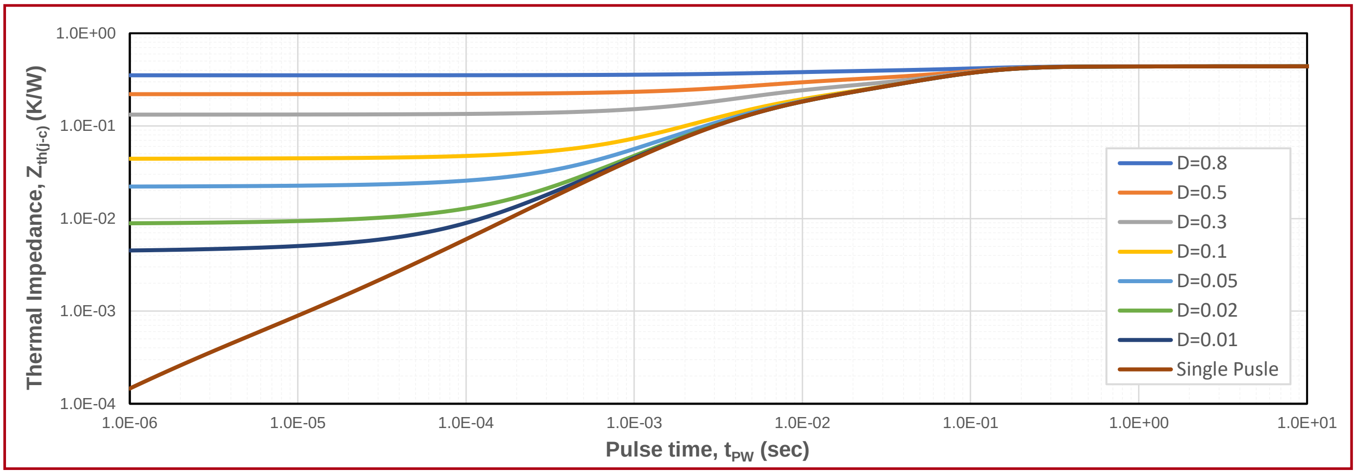


Fig.21 Transient Junction to Case Thermal Impedance

Naming Rule

H2 M 120 Q 040

Generation
H2 = 2^{nd} Gen Discrete

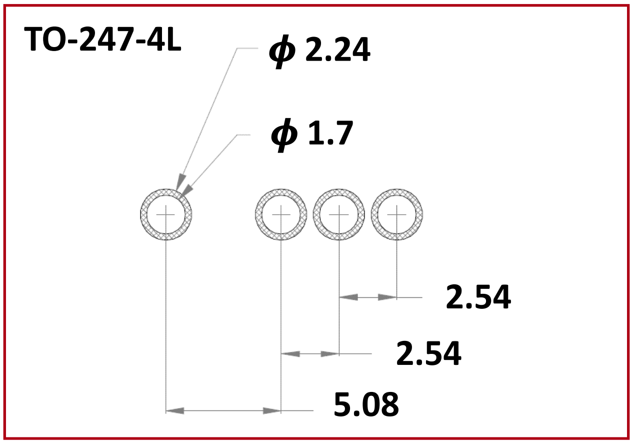
Device Type
M = MOSFET J = JMOS
S = JBS diode

Breakdown Voltage
065 = 650V 170 = 1700V
120 = 1200V 330 = 3300V

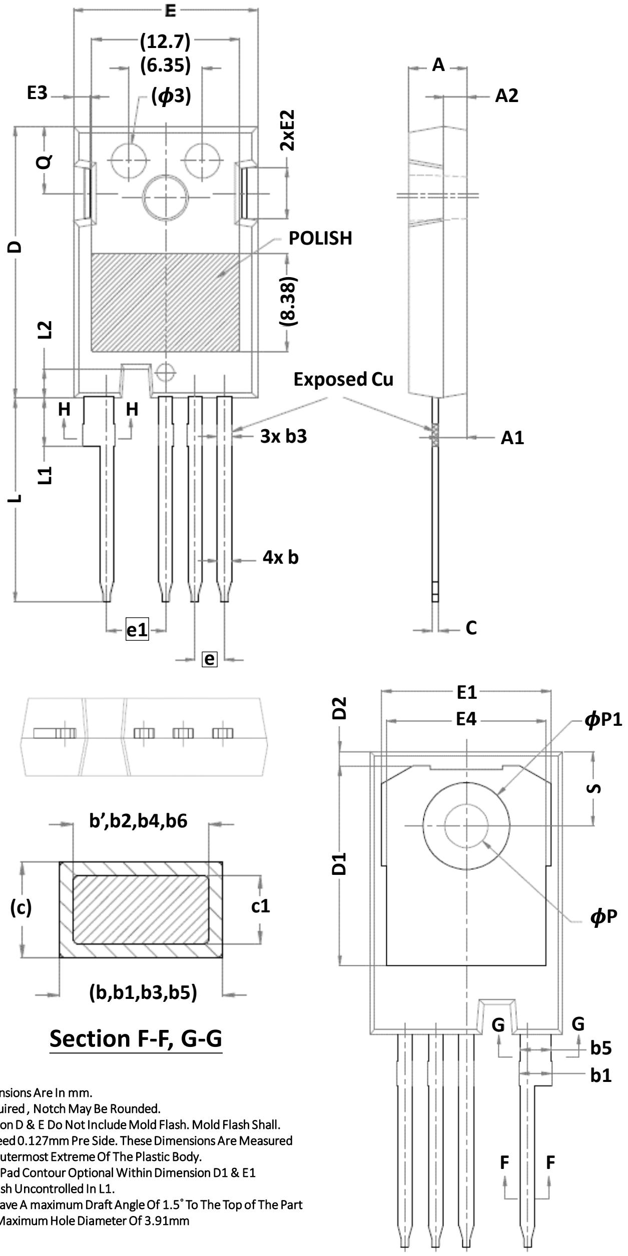
Package
Q = TO-247-4L F = TO-247-3L
B = TO-220-3L T = TO-263-2L

Typical On-Resistance
030 = 30mΩ 040 = 40mΩ 060 = 60mΩ
120 = 120mΩ 240 = 240mΩ

Recommended Solder Pad Layout



Package Dimensions



Section F-F, G-G

Note:
1.All Dimensions Are In mm.
2.Slot Required , Notch May Be Rounded.
3. Dimension D & E Do Not Include Mold Flash. Mold Flash Shall. Not Exceed 0.127mm Pre Side. These Dimensions Are Measured At The outermost Extreme Of The Plastic Body.
4.Thermal Pad Contour Optional Within Dimension D1 & E1
5.Lead Finish Uncontrolled In L1.
6. ϕP To Have A maximum Draft Angle Of 1.5° To The Top of The Part With A Maximum Hole Diameter Of 3.91mm

Symbol	mm		
	Min.	Typ.	Max.
A	4.83	5.02	5.21
A1	2.29	2.41	2.54
A2	1.91	2.00	2.16
b'	1.07	1.20	1.28
b	1.07	1.20	1.33
b1	2.39	2.67	2.94
b2	2.39	2.67	2.84
b3	1.07	1.30	1.60
b4	1.07	1.30	1.50
b5	2.39	2.53	2.69
b6	2.39	2.53	2.64
c	0.55	0.60	0.68
c1	0.55	0.60	0.65
D	23.30	23.45	23.60
D1	16.25	16.55	17.65
D2	0.95	1.19	1.25
E	15.75	15.94	16.13
E1	13.10	14.02	14.15
E2	3.68	4.40	5.10
E3	1.00	1.45	1.90
E4	12.38	13.26	13.43
e	2.54 BSC		
e1	5.08 BSC		
L	17.31	17.57	17.82
L1	3.97	4.19	4.37
L2	2.35	2.50	2.65
ϕP	3.51	3.61	3.65
ϕP1	7.19 REF.		
Q	5.49	5.79	6.00
S	6.04	6.17	6.30

Notes

- The information provided herein is subject to change without notice.
- For other information that does not show on this datasheet, please contact us for inquiry.