DX65B200 E-mode 650V,10A,200mΩ GaN HEMT

1. Features

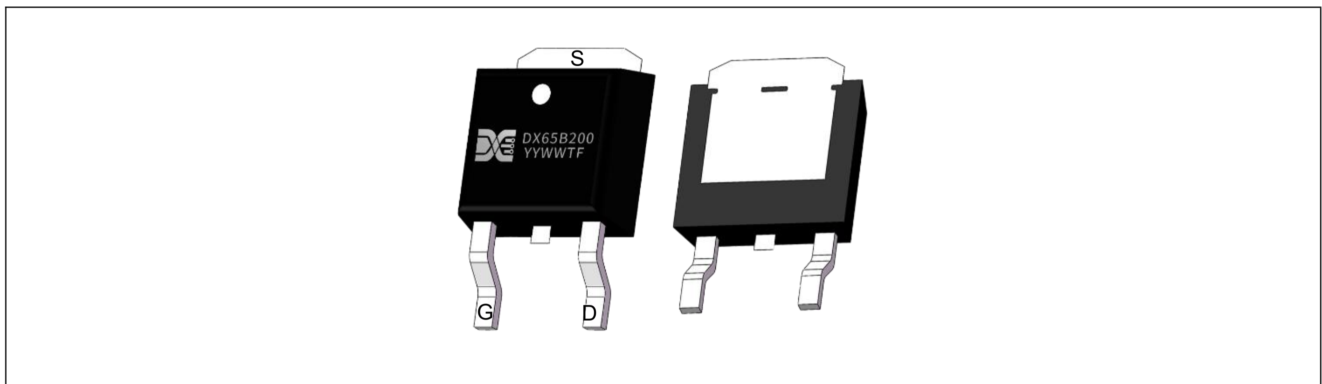
- 650 V enhancement mode power switch
- Easy gate drive requirements
- Very high switching frequency
- Fast and controllable fall and rise times
- Zero reverse recovery loss

2. Key performance parameters

Parameter	Value	Unit
VDS,max	650	V
RDS(on),max@VGS=6V	200	mΩ
QG,typ@VDS=400V	2.4	nC
ID	10	A

3. Device Information

Part Number	Package	Packing
DX65B200	TO252	Tape 2500/reel



4. Applications

- Fast Battery Charging
- Power Factor Correction
- Wireless Power Transfer
- LED lighting drivers
- LLC Converters

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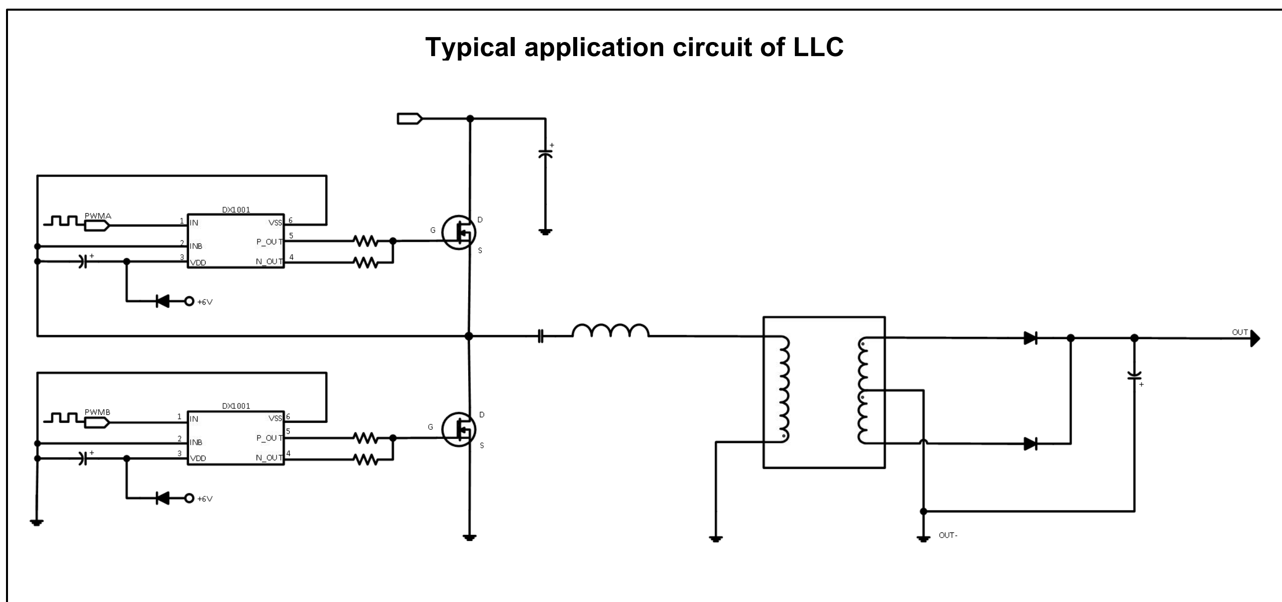
5. Description

DX65B200 is an enhancement mode GaN-on-silicon transistor. GaN is a wide band gap semiconductor with high power density. The gallium nitride transistor is characterized by no body diode, so the reverse recovery charge is zero. This GaN FET is a high performance e-Mode GaN FET that achieves excellent high-frequency and high efficiency operation. Features include a simple gate input and a Source Kelvin pin for noise immunity. This GaN power FET combines the highest dV/dt immunity and industry-standard low-profile, lowinductance, bottom-side cooled SMT QFN packaging to enable designers to achieve simple, quick and reliable solutions.

6. Absolute Maximum Ratings (Tc=25℃ unless otherwise specified)

PARAMETER	SYMBOL	VALUE	UNIT	Condition
Drain-Source voltage	V_{DS}	650	V	
Gate-source voltage	V_{GS}	-1.4 to 7	V	
Continuous drain current*	I_D	10	A	Tc=25℃
Operation and storage temperature	Tj	-55 to 150	℃	
	Tstg	-55 to 150	℃	

* An Estimated Value



Typical application circuit of LLC

7. Electrical Characteristics (Tc=25℃ unless otherwise specified)

7.1 Typical Performance – Static

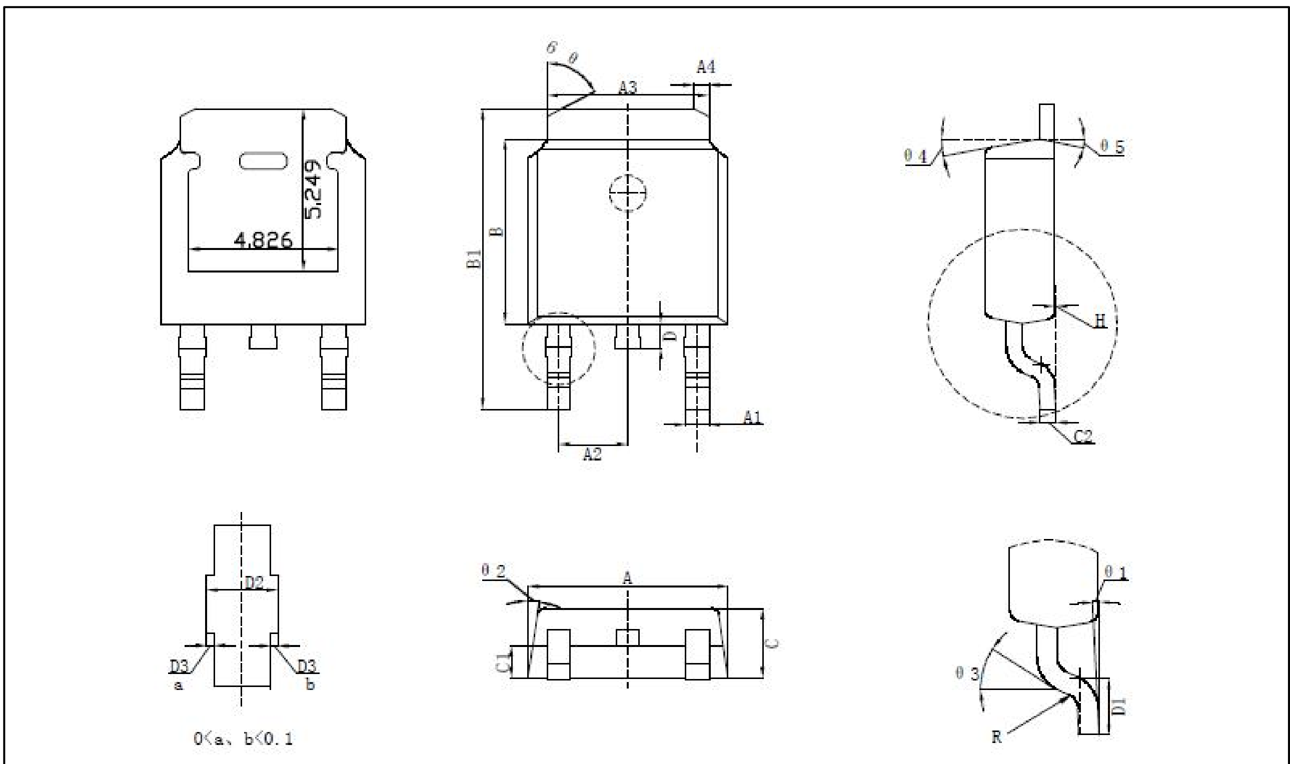
Parameter	Symbol	Value			Unit	Test condition
		Min.	Type.	Max.		
Drain source breakdown. voltage	BV_{DS}	650	/	/	V	VGS=0V, ID=20μA
Total drain leakage current	I_{DSS}	/	1	10	μA	VDS=650V, VGS=0V, Tj=25℃
		/	8	110	μA	VDS=650V, VGS=0V, Tj=150℃
Gate-to-source current	I_{GSS}	/	10	/	μA	VDS=0V, VGS=6V, Tj=25℃
Total gate charge	$R_{DS(ON)}$	/	150	200	mΩ	VGS=6V, ID=3A, Tj=25℃
		/	300	/	mΩ	VGS=6V, ID=3A, Tj=150℃
Gate threshold voltage	$V_{GS(th)}$	1.2	1.6	2.5	V	VDS=VGS, ID=11mA,

7.2 Typical Performance – Dynamic

Parameter	Symbol	Value			Unit	Test condition
		Min.	Type.	Max.		
Input capacitance	C_{ISS}	/	72	/	pF	VDS=400V,VGS=0V,f=1MHz
Output capacitance	C_{OSS}	/	20	/	pF	
Reverse transfer capacitance	C_{RSS}	/	0.2	/	pF	
Output capacitance, energy related	$C_{OSS(er)}$	/	31	/	pF	VDS=0V to 400V,VGS=0V
Output capacitance time related	$C^{OSS(tr)}$	/	44	/	pF	
Total gate charge	Q_G	/	2.4	/	nC	VDS=400V, VGS=0V to 6V
Gate-drain charge	Q_{GD}	/	1.1	/	nC	
Gate-source charge	Q_{GS}	/	0.25	/	nC	
Gate Resistance	R_G	/	1.95	/	Ω	f = fres, Open drain

8. Package

尺寸 / 标注	最小(㎜)	最大(㎜)	尺寸 / 标注	最小(㎜)	最大(㎜)
A	6.50	6.70	D1	1.40	1.60
A1	0.71	0.81	D2	0.81	0.91
A2	2.236	2.336	D3	0.05TYP	
A3	5.284	5.384	H	0.00	0.10
A4	0.75	0.85	R	0.40TYP	
B	6.00	6.20	θ1	0° — 8°	
B1	9.80	10.10	θ2	8.5°TYP4	
C	2.20	2.40	θ3	25°TYP	
C1	0.967	1.087	θ4	10°TYP2	
C2	0.498	0.518	θ5	10°TYP	
D	0.70	0.90	θ6	70°TYP	



9. Packing

ITEM	W	A_O	B_O	B_1	B_2	K_O	K_1	E	F	D_1	D_0	P_0	P_1	P_2	t
MIN	16.30	6.80	10.40	2.15	7.50	2.50	0.65	1.65	7.45	—	—	3.90	7.90	1.90	0.20
NOM	16.00	6.90	10.50	2.20	7.55	2.60	0.70	1.75	7.50	1.50	1.50	4.00	8.00	2.00	0.25
MAX	15.90	7.00	10.60	2.25	7.60	2.70	0.75	1.85	7.55	1.60	1.60	4.10	8.10	2.10	0.30