1. 特性

- 符合车规 AEC-Q100 认证
  - 温度等级 1：–40°C 至 125°C 工作环境温度
- 供电电压范围：
  - 工作电压范围：5.5V 至 28V
  - 最高耐压：40V
  - 数字供电支持：1.8V/3.3V/5V
- 支持 3 个 PWM 输入，最高频率超过 25kHz
- 多通道半桥驱动器
  - 8 个半桥驱动最多 16 个外部 NMOS
  - 支持 100% PWM 占空比，
  - 外部 MOS 开关速度自适应控制
- 智能栅极驱动器：驱动能力可配置 1-96mA 可调
- 支持睡眠模式以及低功耗模式
- 24-bit SPI 通讯
- 支持电荷泵展频
- 睡眠模式或者正常模式下支持：4 个低边支持可配置自动刹车
- 支持优化高/低边工作模式
- 集成两路电流检测放大器：
  - 四档增益可调：10/20/40/80V/V
  - 支持 PWM 抑制功能
- 多种保护和诊断功能：
  - VM 过压，欠压保护， 电荷泵欠压保护
  - VDS 过压保护
  - 过温关断和过温报警
  - 支持 Fail-Safe 模式
  - 支持握手逻辑防止上下管穿通
  - 支持看门狗
  - 支持离线负载开路短路诊断

2. 应用

- 汽车电动座椅，电动车门
- 车身控制
- 车上各类直流有刷电机

3. 说明

DR7808Q 是一款多通道栅极驱动器，集成的 8 个半桥最多可驱动 16 个外部 NMOSFET，其广泛用于驱动汽车上各类直流电有刷电机，例如汽车电动座椅，电动车门等。

DR7808Q 支持 24 位串行外设接口(SPI)用于对芯片进行配置或者监。此外，SPI 还可以直接控制半桥。除了 SPI，DR7808Q 还支持 3 路 PWM 输入控制 8 个半桥。

DR7808Q 的八路半桥驱动支持智能栅极驱动技术，可以根据外部 NMOSFET 的参数和应用需求，实现驱动能力 8 档软件可配置，其最大驱动能力 96mA。此外，所有半桥都支持智能自适应开关速度调节。此外，DR7808Q 基于握手逻辑对上下管开关进行保护，可有效防止上下管穿通。

DR7808Q 提供广泛的保护和诊断功能，例如电源电压监控、过流保护、电荷泵电压、温度警告、过热关断看门狗和负载开路短路诊断等。每个栅极驱动器可独立监控其外 MOSFET 漏极-源极电压以发现应用故障。

DR7808Q 支持 7mm x7mm QFN-48 封装。该封装底部带有散热焊盘，可提供良好的热性能并最大限度地减少所需的 PCB 空间。有关订购信息，请参见下表 1。

Table 1 lists the order information.

Table 1. Order Information

ORDER NUMBER(1)	PART NUMBER	PKG.	VM MAX (V)	INTERFACE	BRIDGE	HSD Opt(1)	OP. TEMP (°C)	PKG. OPTION
DR7808QAQFN48	DR7808Q	QFN-48	40	SPI	8	Yes	–40-125	TBD

(1) HSD Opt: high-side driver optimization, low-side of a half bridge can be disabled and then the half bridge can then be used as high side driver.

Table 2. Family Selection Guide

TBD

Note : Available in the future.

Devices can be ordered via the following two ways:

1. Place orders directly on our website (www.analogysemi.com), or;
2. Contact our sales team by mailing to sales@analogysemi.com.

4. PIN CONFIGURATION AND FUNCTIONS

Figure 1 illustrates the pin configuration.

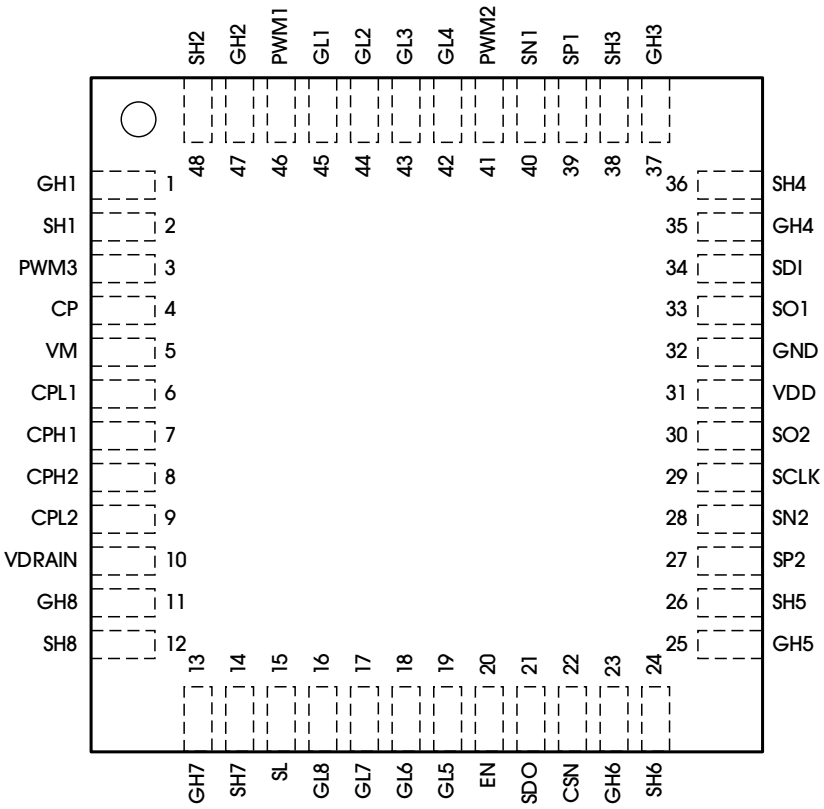


Figure 1. DR7808Q Pin Configuration

Table 3 lists the pin functions.

Table 3. Pin Functions

POSITION	NAME	TYPE	DESCRIPTION
1	GH1	Output	Gate high-side 1 Analog I/O pin to turn on/off high-side MOSFET 1. Connect to the gate of high-side MOSFET 1.
2	SH1	Input	Source high-side 1 Connect to source of high-side MOSFET 1.
3	PWM3	Input	PWM input 3
4	CP	Output	Charge pump output
5	VM	Power	Device supply voltage Connect this pin to the supply (battery) voltage with a reverse battery protection circuit.
6	CPL1	I/O	Negative connection to charge pump capacitor 1
7	CPH1	I/O	Positive connection to charge pump capacitor 1
8	CPH2	I/O	Positive connection to charge pump capacitor 2
9	CPL2	I/O	Negative connection to charge pump capacitor 2
10	VDRAIN	Input	Drain input for high-sides Input for the drains of high-side MOSFETs.
11	GH8	Output	Gate high-side 8
12	SH8	Input	Source high-side 8
13	GH7	Output	Gate high-side 7
14	SH7	Input	Source high-side 7

POSITION	NAME	TYPE	DESCRIPTION
15	SL	Input	Source low-side Common connection to the source of the low-side MOSFETs.
16	GL8	Output	Gate low-side 8
17	GL7	Output	Gate low-side 7
18	GL6	Output	Gate low-side 6
19	GL5	Output	Gate low-side 5
20	EN	Input	Enable input with internal pull-down
21	SDO	Output	Serial data output
22	CSN	Input	Chip select (without internal pull-up)
23	GH6	Output	Gate high-side 6
24	SH6	Input	Source high-side 6
25	GH5	Output	Gate high-side 5
26	SH5	Input	Source high-side 5
27	SP2	Input	Non-Inverting input of current sense amplifier 2
28	SN2	Input	Inverting input of current sense amplifier 2
29	SCLK	Input	Serial clock input with internal pull-down
30	SO2	Output	Current sense amplifier output 2
31	VDD	Power	Logic supply
32	GND	Ground	Ground connection
33	SO1	Output	Current sense amplifier output 1
34	SDI	Input	Serial data input with internal pull-down
35	GH4	Output	Gate high-side 4
36	SH4	Input	Source high-side 4
37	GH3	Output	Gate high-side 3
38	SH3	Input	Source high-side 3
39	SP1	Input	Non-inverting input of current sense amplifier 1
40	SN1	Input	Inverting input of current sense amplifier 1. This pin can be used as reference for the high-side MOSFET drain if current sense amplifier 1 is configured as the high side.
41	PWM2	Input	PWM input 2
42	GL4	Output	Gate low-side 4
43	GL3	Output	Gate low-side 3
44	GL2	Output	Gate low-side 2
45	GL1	Output	Gate low-side 1
46	PWM1	Input	PWM input 1
47	GH2	Output	Gate high-side 2
48	SH2	Input	Source high-side 2
—	E.P.	—	Exposed pad For cooling purpose only, do not use as electrical GND(1).

Note: The exposed pad at the bottom of the package allows better power dissipation from DR7808Q via the PCB. The exposed pad must be left floating or connected to GND (recommended) for the best EMC and thermal performance.

5. SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS

Table 4 lists the absolute maximum ratings of the DR7808Q .

Table 4. Absolute Maximum Ratings

PARAMETER	DESCRIPTION		MIN	MAX	UNITS
Voltage	Supply voltage	VM	–0.3	40	V
	PWM input voltages (PWMx)	VPWMx	–0.3	VDD + 0.3	
	Logic input voltages (SDI, SCLK, CSN, EN)	VSDI, VSCLK, VCSN, VEN	–0.3	VDD + 0.3	
	Voltage range and SDO	VSDO	–0.3	VDD + 0.3	
	Voltage range at SPx and SNx	VSP, VSN	–5.0	40	
	Differential input voltage range SPx - SNx	VCSIDiff	–8.0	8.0	
	Voltage range at VDRAIN	VDRAIN	–0.3	40	
	Voltage range at SL	VSL	–5.0	6.0	
	Voltage range at SHx	VSH	–5.0	48	
	Voltage range at GHx	VGH	–5.0	48	
	Voltage range at GLx	VGL	–5.0	20	
	Voltage difference between GLx and SL	VGS_LS	–0.3	16	
	Voltage difference between GHx and SHx	VGS_HS	–0.3	16	
	Voltage range at charge pump pins CP, CPH1， CPH2	VCP	– 0.3	VM + 12	
	Voltage range at charge pump pins CPL1, CPL2	VCPCx	– 0.3	VM	
	Logic supply voltage	VDD	–0.3	5.5	
	Voltage at SOx	VSOx	–0.3	VDD + 0.3	
Current	Shunt amplifier output pin	SO1, SO2	0	5	mA
	Maximum, limit with external series resistor	VDRAIN	–2	2	
	Gate pin source	GHx, GLx	0	200	
	Gate pin sink	GHx, GLx	0	200	
Temperature	Junction, T_J		–40	150	°C
	Storage, T_{stg}		–55	150	

Note: Stresses beyond those listed under Table 4 may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Table 6. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD RATINGS

Table 5 lists the ESD ratings of the DR7808Q .

Table 5. ESD Ratings

PARAMETER	SYMBOL	DESCRIPTION	VALUE	UNITS
Electrostatic Discharge	$V_{(ESD)}$	Human-body model (HBM), per AEC Q100-002	TBD	V
		Charged-device model (CDM), per AEC Q100-011	TBD	

5.3 RECOMMENDED OPERATING CONDITIONS

Table 6 lists the recommended operating conditions for the DR7808Q .

Table 6. Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage Range for Normal Operation		5.5	28	V
Extended Supply Voltage Range		28	36	V
Logic Supply Voltage		3	5.5	
SPI Logic Input Voltage		0	VDD	
Applied PWM Signal (IN1/IN2), IN1, IN2	$f_{(PWM)}$		25	kHz
Shunt Amplifier Output-Current Loading, SO	I_{SO}		5	mA
Operating Ambient Temperature	T_J	–40	150	°C

5.4 THERMAL INFORMATION

Table 7 lists the thermal information for the DR7808Q .

Table 7. Thermal Information

PARAMETER	SYMBOL	TBD	UNITS
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	TBD	°C/W
Junction-to-Board Thermal Resistance	$R_{\theta JB}$	TBD	°C/W
Junction-to-Top Characterization Parameter	ψ_{JT}	TBD	°C/W
Junction-to-Board Characterization Parameter	ψ_{JB}	TBD	°C/W
Junction-to-Case (Top) Thermal Resistance	$R_{\theta JC\ (top)}$	TBD	°C/W
Junction-to-Case (Bottom) Thermal Resistance	$R_{\theta JC\ (bot)}$	TBD	°C/W

5.5 ELECTRICAL CHARACTERISTICS

5.5.1 SUPPLY

Table 8 lists the electrical characteristics (supply) of DR7808Q . VM = 6.0V to 18V if VSOVTH = 0, VM = 6.0V to 28V if VSOVTH = 1; V_{DD} = 3.0V to 5.5V, T_J = –40°C to 150°C, all voltages with respect to ground, positive current flowing into pin, unless otherwise specified.

Table 8. Electrical Characteristics (Supply)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT CONSUMPTION, EN = LOW						
Supply Quiescent Current (VM + VDRAIN)	I_{SQ}	T_J < 85°C, VM = 13.5V		6		μA
	I_{SQ2}	T_J < 85°C, VM < 25V			TBD	μA
Logic Supply Quiescent Current	I_{DD_Q}	T_J < 85°C		0.5		μA
Total Quiescent Current	I_{DD_Q} + I_{SQ}	T_J < 85°C, VM = 13.5V		6.5		μA
EN Low Filter Time	t_{DSLEEP}	(2) (3) BD_PASS = 0		Max. t_{CCP} + 3		μs
EN Low Filter Time	t_{ENL_FILT}	(2)		2.5		μs
VM for LS1-4 Setting	V_{SLEEP_SET}			3.7		V
CURRENT CONSUMPTION, EN = HIGH						
Supply (VM + VDRAIN) Current at Active Mode	I_{S1}	8V < VM < 28V, HBxMODE = 00B/11B, BD_PASS = 0, DRV_LPWR_EN = 0		19.7		mA
	$I_{S1\_BD\_PASS}$	8V < VM < 28V, HBxMODE = 00B/11B, BD_PASS = 1, DRV_LPWR_EN = 0		0.33		mA
	I_{S2}	8V < VM < 28V, HBxMODE = 00B/11B, BD_PASS = 0, DRV_LPWR_EN = 1		8.5		mA
	$I_{S2\_BD\_PASS}$	8V < VM < 28V, HBxMODE = 00B/11B, BD_PASS = 1, DRV_LPWR_EN = 1		0.32		mA
Supply (VDD) Current at Active Mode	I_{DD1}	HBxMODE = 00B/11B, BD_PASS = 0, CSA1 and CSA2 off		10.4		mA
	I_{DD2}	HBxMODE = 00B/11B, BD_PASS = 0, CSA1 and CSA2 on		7.4		mA
VM WITH ACTIVE BRIDGE DRIVER, BD_PASS = 0						
UV Switch ON Voltage	$V_{SUV\ ON}$	VM increasing			5.5	V
UV Switch OFF Voltage	$V_{SUV\ OFF}$	VM decreasing	4.0	4.5	5.0	V
UV ON/OFF Hysteresis	$V_{SUV\ HY}$	$V_{SUV\ ON}$ – $V_{SUV\ OFF}$ (2)		0.5		V
OV Switch OFF Voltage VSOVTH = 0	$V_{SOV\ OFF1}$	VM increasing		20.2		V
OV Switch ON Voltage VSOVTH = 0	$V_{SOV\ ON1}$	VM decreasing		19.4		V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OV Switch OFF Voltage VSOVTH = 1	$V_{SOV\ OFF2}$	VM increasing		30.2		V
OV Switch ON Voltage VSOVTH = 1	$V_{SOV\ ON2}$	VM decreasing		29		V
OV ON/OFF Hysteresis	$V_{SOV\ HY}$	$V_{SUV\ ON} - V_{SUV\ OFF}$		1		V
VM Undervoltage Filter Time	t_{VSUV_FILT}	(1)		10		µs
VM Overvoltage Filter Time	t_{VSOV_FILT}	(2)		10		µs
CP Turn-Off Delay After VM Overvoltage Detection	t_{D_CPVSOV}	(2)		16		µs
V_{DD}						
V_{DD} Power-On-Reset	$V_{DD\ POR}$	V_{DD} increasing		2.6		V
V_{DD} Power-Off-Reset	$V_{DD\ POffR}$	V_{DD} decreasing		2.4		V
V_{DD} Power-On-Reset Hysteresis	$V_{DD\ POR\ HY}$	$V_{DD\ POR} - V_{DD\ POffR}$		0.2		V

Note 1: Additional quiescent current if VM drops below V_{SLEEP_SET}.
Note 2: Not subject to production test, specified by design.
Note 3: Max. cross-current protection time of the active half-bridges.
Note 4: Parameter independent of VSOVTH.
Note 5: Parameter independent of CCSO.

5.5.2 LOGIC INPUTS PWM$_x$, EN

Table 9 lists the electrical characteristics (logic inputs PWMx, EN) of DR7808Q . VM = 6.0V to 18V if VSOVTH = 0, VM = 6.0V to 28V if VSOVTH = 1; V_{DD} = 3.0V to 5.5V, T_J = –40°C to 150°C, all voltages with respect to ground, positive current flowing into pin, unless otherwise specified.

Table 9. Electrical Characteristics (Logic Inputs PWMx, EN)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EN High Voltage	V_{ENH}		0.7 × V_{DD}			V
EN Low Voltage	V_{ENL}				0.3 × V_{DD}	V
EN Hysteresis	V_{ENHY}	(1)		0.12 × V_{DD}		V
EN Pull-Down Resistor	R_{PD_EN}		30	40	50	kΩ
PWMx High Voltage	V_{PWMH}		0.7 × V_{DD}			V
PWMx Low Voltage	V_{PWML}				0.3 × V_{DD}	V
PWMx Hysteresis	V_{PWMHY}	(1)		0.12 × V_{DD}		V
PWMx Pull-Down Resistor	R_{PD_PWMx}		30	40	50	kΩ

Note: Not subject to production test, specified by design.

5.5.3 CHARGE PUMP

Table 10 lists the electrical characteristics (charge pump) of DR7808Q . VM = 6.0V to 18V if VSOVTH = 0, VM = 6.0V to 28V if VSOVTH = 1; V_{DD} = 3.0V to 5.5V, T_J = –40°C to 150°C, all voltages with respect to ground, positive current flowing into pin, unless otherwise specified.

Table 10. Electrical Characteristics (Charge Pump)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Charge Pump Frequency	f_{CP}	(3)		250		kHz
Output Voltage VCP VM. VM	V_{CPmin}	VM = 6V, I_{CP} = –6mA		8.7		V
Regulated Output Voltage VCP VM. VM, CPSTGA = 0	V_{CP1}	8V < VM < 28V, I_{CP} = –12mA		10.5		V
Regulated Output Voltage VCP VM. VM, CPSTGA = 1	V_{CP2}	18V < VM < 28V, I_{CP} = –12mA		10.5		V
Turn-On Time, CPSTGA = 0	t_{ON_VCP1}	8V < VM < 28V (25%)(1) (2) (3) (4)		9		µs
Rise Time, CPSTGA = 0	t_{RISE_VCP1}	8V < VM < 28V (25%-75%)(1) (2) (3) (4)		46		µs

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Turn-On Time, CPSTGA = 1	t_{ON_VCP2}	18V < VM < 28V (25%)(1) (2) (3) (5)		8		μs
Rise Time, CPSTGA = 1	t_{RISE_VCP2}	18V < VM < 28V (25%-75%)(1) (2) (3) (5)		20		μs
Charge Pump Undervoltage (Referred to VM)	V_{CPUV1}	CPUVTH = 0, VCP falling		6		V
	V_{CPUV2}	CPUVTH = 1, VCP falling		7.5		V
Automatic Switch Over Dual to Single Stage Charge Pump	$V_{CPSO\ DS}$	CPSTGA = 1		17		V
Automatic Switch Over Single to Dual Stage Charge Pump	$V_{CPSO\ SD}$	CPSTGA = 1		16.5		V
Charge Pump Switch Over Hysteresis	$V_{CPSO\ HY}$	(3) CPSTGA = 1, $V_{CPSO\ DS} - V_{CPSO\ SD}$		0.7		V
Charge Pump Undervoltage Filter Time	t_{CPUV}	(3)		32		μs
Charge Pump Minimum Output Current	I_{CPOC1}	(2) (3) (4) VM = 13.5V; CPSTGA = 0			–12	mA
	I_{CPOC2}	(2) (3) (5) VM = 18V; CPSTGA = 1			–12	mA

Note 1: Parameter dependent on the capacitance C_{CP}.
Note 2: $C_{CPC1} = C_{CPC2} = 220nF$, $C_{CP} = 470nF$, $I_{CP} = 0mA$.
Note 3: Not subject to production test, specified by design.
Note 4: Dual stage charge pump.
Note 5: Single stage charge pump.

5.5.4 GATE DRIVER

Table 11 lists the electrical characteristics (gate driver) of DR7808Q . VM = 6.0V to 18V if VSOVTH = 0, VM = 6.0V to 28V if VSOVTH = 1; V_{DD} = 3.0V to 5.5V, T_J = –40°C to 150°C, V_{CP} > VM + 8.5V, all voltages with respect to ground. Positive current flowing into pin except for I_{GLx} and I_{GHx}, unless otherwise specified.

Table 11. Electrical Characteristics (Gate Driver)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
COMPARATORS						
SHx High Threshold	V_{SHH}		VM – 2.5		VM – 2.0	V
SHx Low Threshold	V_{SHL}	Referred to GND	2		2.5	V
MOSFET DRIVER OUTPUT						
High Level Output Voltage, GHx VM. SHx, CPSTGA = 0	V_{GH1_HS}	VM > 8V, C_{Load} = 10nF, I_{CP} = –12mA (2)		10.1		V
High Level Output Voltage, GLx VM. SL, CPSTGA = 0	V_{GH1_LS}	VM > 8V, C_{Load} = 10nF, I_{CP} = –12mA (2)		10.1		V
High Level Output Voltage, GLx VM. SL, CPSTGA = 0	V_{GH2_HS}	VM > 6V, C_{Load} = 10nF, I_{CP} = –6mA (2)		8.2		V
High Level Output Voltage, GHx VM. SHx, CPSTGA = 0	V_{GH2_LS}	(1) VM > 6.0V, C_{Load} = 10nF, I_{CP} = –6mA (2)		7		V
High Level Output Voltage GHx VM. SHx and GLx VM. SL, CPSTGA = 1	V_{GH4}	(1) VM > 18V, C_{Load} = 10nF, I_{CP} = –12mA (2)		10.5		V
Charge Current	I_{CHG0}	I_{CHG} = 0D, C_{Load} = 10nF, VCP-GHx > 2V		1.0		mA

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
	I_{CHG6}	I_{CHG} = 6D, C_{Load} = 10nF, VCP-GHx > 2V		9.0		mA
	I_{CHG14}	I_{CHG} = 14D, C_{Load} = 10nF, VCP-GHx > 5V		30.0		mA
Charge Current	I_{CHG30}	I_{CHG} = 30D, C_{Load} = 10nF, VCP-GHx > 5V		96		mA
Discharge Current	I_{DCHG0}	I_{DCHG} = 0D, C_{Load} = 10nF, GLx-SL > 2V		–1.0		mA
	I_{DCHG6}	I_{DCHG} = 6D, C_{Load} = 10nF, GLx-SL > 2V		–9.4		mA
	I_{DCHG14}	I_{DCHG} = 14D, C_{Load} = 10nF, GLx-SL > 5V		–32.0		mA
	I_{DCHG30}	I_{DCHG} = 30D, C_{Load} = 10nF, GLx-SL > 5V		–95		mA
Passive Discharge Resistance Between GHx/GLx and GND	R_{GGND}	(1)		5.7		kΩ
Passive Discharge Resistance Between GL1-4 and GND	R_{GGND}			54		Ω
GATE DRIVERS DYNAMIC PARAMETERS						
PWM Synchronization Delay	t_{PWM_SYNCH}	(1)	50		150	ns
Pre-Charge Time	t_{PCHG00}	(1)TPCHG = 00B		125		ns
	t_{PCHG01}	(1) TPCHG = 01B		250		ns
	t_{PCHG10}	(1) TPCHG = 10B		500		ns
	t_{PCHG11}	(1) TPCHG = 11B		1000		ns
Pre-Discharge Time	$t_{DPCHG00}$	(1) TDPCHG = 00B		125		ns
	$t_{DPCHG01}$	(1) TDPCHG = 01B		250		ns
	$t_{DPCHG01}$	(1) TDPCHG = 10B		500		ns
	$t_{DPCHG01}$	(1) TDPCHG = 11B		1000		ns

Note 1: Not subject to production test, specified by design.
Note 2: ICHGx(4:0) = 11111B (100mA typ.)

5.5.5 PROTECTIONS AND DIAGNOSTICS

The specified drain-source monitoring thresholds, the overcurrent thresholds, and the electrical characteristics related to the current sense amplifiers are valid for V_{CP} > VM + 8V.

Table 12 lists the electrical characteristics (protections and diagnostics) of DR7808Q . VM = 6.0V to 18V if VSOVTH = 0, VM = 6.0V to 28V if VSOVTH = 1; V_{DD} = 3.0V to 5.5V, T_J = –40°C to 150°C, V_{CP} > VM + 8V, all voltages with respect to ground. Positive current flowing into pin, unless otherwise specified.

Table 12. Electrical Characteristics (Protections and Diagnostics)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
WATCHDOG						
Watchdog Period 1	T_{WDPER1}	(1) WDPER = 0		50		ms
Watchdog Period 2	T_{WDPER2}	(1) WDPER = 1		200		ms
OFF-STATE OPEN LOAD DIAGNOSIS						
Pull-Up Diagnosis Current	I_{PUDiag}	(1)		–500		μA
Pull-Down Diagnosis Current	I_{PDDiag}	(1)		1000		μA
Diagnostic Current Ratio	I_{Diag_ratio}	Ratio IPDDiag/IPUDiag		2		
DRAIN SOURCE MONITORING THRESHOLD						

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Drain-Source Monitoring Thresholds	$V_{VDSMONTH0}$	HBxVDSTH(2:0) = 000B, reg_default		0.15		V
	$V_{VDSMONTH1}$	HBxVDSTH(2:0) = 001B, reg_default		0.20		V
	$V_{VDSMONTH2}$	HBxVDSTH(2:0) = 010B, reg_default		0.25		V
	$V_{VDSMONTH3}$	HBxVDSTH(2:0) = 011B, reg_default		0.30		V
	$V_{VDSMONTH4}$	HBxVDSTH(2:0) = 100B, reg_default		0.40		V
	$V_{VDSMONTH5}$	HBxVDSTH(2:0) = 101B, reg_default		0.50		V
Drain-Source Monitoring Thresholds	$V_{VDSMONTH6}$	HBxVDSTH(2:0) = 110B, reg_default		0.60		V
	$V_{VDSMONTH7}$	HBxVDSTH(2:0) = 111B, reg_default		2.0		V
	$V_{VDSMONTH0}$	HBxVDSTH(2:0) = 000B, reg_self_define_enable		0.075		V
	$V_{VDSMONTH1}$	HBxVDSTH(2:0) = 000B, reg_self_define_enable		0.1		V
	$V_{VDSMONTH2}$	HBxVDSTH(2:0) = 000B, reg_self_define_enable		0.125		V
	$V_{VDSMONTH3}$	HBxVDSTH(2:0) = 000B, reg_self_define_enable		0.15		V
	$V_{VDSMONTH4}$	HBxVDSTH(2:0) = 000B, reg_self_define_enable		0.2		V
	$V_{VDSMONTH5}$	HBxVDSTH(2:0) = 000B, reg_self_define_enable		0.25		V
	$V_{VDSMONTH6}$	HBxVDSTH(2:0) = 000B, reg_self_define_enable		0.3		V
	$V_{VDSMONTH7}$	HBxVDSTH(2:0) = 000B, reg_self_define_enable		1		V
	$V_{VDSMONTH7}$	HBxVDSTH(2:0) = 111B		2		V
DRAIN-SOURCE MONITORING BLANK TIME						
DS Monitoring Blank Time	t_{DSMON_BLK0}	TBLANKx(2:0) = 000B(1)		625		ns
	t_{DSMON_BLK1}	TBLANKx(2:0) = 001B(1)		1		µs
	t_{DSMON_BLK2}	TBLANKx(2:0) = 010B(1)		1.25		µs
	t_{DSMON_BLK3}	TBLANKx(2:0) = 011B(1)		1.5		µs
	t_{DSMON_BLK4}	TBLANKx(2:0) = 100B(1)		2		µs
	t_{DSMON_BLK5}	TBLANKx(2:0) = 101B(1)		3		µs
	t_{DSMON_BLK6}	TBLANKx(2:0) = 110B(1)		4		µs
	t_{DSMON_BLK7}	TBLANKx(2:0) = 111B(1)		16		µs
DRAIN-SOURCE MONITORING FILTER TIME						
DS Monitoring Filter Time	t_{DSMON_FILT0}	TFVDS(1:0) = 00B(1)		0.5		µs
	t_{DSMON_FILT1}	TFVDS(1:0) = 01B(1)		1		µs
	t_{DSMON_FILT2}	TFVDS(1:0) = 10B(1)		2		µs
	t_{DSMON_FILT3}	TFVDS(1:0) = 11B(1)		3		µs
CROSS-CURRENT PROTECTION TIME						
Dead Time	$t_{HBxCCP0}$	THBxCCP(2:0) = 000B(1)		375		ns
	$t_{HBxCCP1}$	THBxCCP(2:0) = 001B(1)		625		ns
	$t_{HBxCCP2}$	THBxCCP(2:0) = 010B(1)		1		µs
	$t_{HBxCCP3}$	THBxCCP(2:0) = 011B(1)		1.5		µs
	$t_{HBxCCP4}$	THBxCCP(2:0) = 100B(1)		2		µs

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
	$t_{HBxCCP5}$	THBxCCP(2:0) = 101B(1)		3		µs
	$t_{HBxCCP6}$	THBxCCP(2:0) = 110B(1)		4		µs
	$t_{HBxCCP7}$	THBxCCP(2:0) = 111B(1)		16		µs
BRIDGE DRIVER PASSIVE MODE: BD_PASS = 1 AND ALL HBXMODE(1:0) = 00B OR 11B, OR EN = LOW OR $V_{DD} < V_{DD\ POR}$						
Passive VM Overvoltage	$V_{SOV\ PASS\ OFF}$	VM increasing, PASS_MOD = 10B		32.5		V
Passive VM Overvoltage Hysteresis	$V_{SOV\ PASS\ HY}$	(1)		2.5		V
PWM3 Open Drain Resistance	R_{PWM3_OD}			5.5		kΩ
Passive Turn-On Time	$t_{ON\_BD\_PASS}$	(1) Cap = 10nF, VCap = 5V, VM > 8V		4.5		µs
Passive Turn-Off Time	$t_{OFF\_BD\_PASS}$	(1) Cap = 10nF, VCap down to 1.5V, VM > 8V		0.7		µs
Passive LS Gate Voltage	V_{GLx_BRAKE}	VGLx – VSL, x = 1 to 4, VM > 8V		7		V
Passive Turn-On Blank Time	$t_{BLK\_BD\_PASS}$	(1)		6		µs
PWM1 High Voltage, Bridge Driver Passive	$V_{PWM1H\_BD\_PASS}$			1.3		V
Passive VDS Filter Time	$t_{DSMON\_FILT\_BD\_PASS}$	(1)		1		µs
Passive Drain-Source Monitoring Thresholds	$V_{VDSMON\_BD\_PASS}$	PASS_VDS = 1B		0.37		V
CURRENT SENSE AMPLIFIER						
Operating Common Mode Input Voltage Range Referred to GND (CSIPx – GND) or (CSINx – GND)	V_{CM}		–4		28	V
Common Mode Rejection	CMRR	DC, V_{CM} = –4V to 40V,(1) $V_{CSIPx} = V_{CSINx}$, CSAG = (0, 0)/(01)/(10)/11		130		dB
		DC to 50kHz, V_{CM} = –4V … 40V,(1) $V_{CSIPx} = V_{CSINx}$, CSAG = (0, 0)		TBD		dB
Settling Time to 98%	t_{SET}	(1)		1500		ns
Settling Time to 98% After Gain Change	t_{SET_GAIN}	(1) After gain change from CSN rising edge		1300		ns
Input Offset Voltage	V_{OS}			-0.3		mV
Current Sense Amplifier DC Gain (Uncalibrated)	G_{DIFF10}	CSAG = (0, 0)		10		V/V
	G_{DIFF20}	CSAG = (0, 1)		20		V/V
	G_{DIFF40}	CSAG = (1, 0)		40		V/V
	G_{DIFF80}	CSAG = (1, 1)		80		V/V
Gain Drift	G_{DRIFT}	(1) Gain drift after calibration	–0.15		0.5	%
CSOx Single Ended Output Voltage Range (Linear Range)	V_{CSOx}	(1)	0.5		V_{DD} – 0.5	V
Reference Voltage for Unidirectional CSAx	$V_{REF\ Unidir}$	CSDx = 0, $V_{CSIPx} = V_{CSINx}$	–1.5	VDD / 5	0.01	V
Reference Voltage for Bidirectional CSAx	$V_{REF\ Bidir}$	CSDx = 1, $V_{CSIPx} = V_{CSINx}$	–1%	VDD / 2	0.01	V
OVERCURRENT DETECTION						
Overcurrent Filter Time	t_{FOC}	OCxFILT = 00B		6		µs
		OCxFILT = 01B		10		µs
		OCxFILT = 10B		50		µs
		OCxFILT = 11B(1) (2)		100		µs

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OC Threshold (CSIP-CSIN), Unidirectional	$V_{OCTH1\ Unidir}$	CSDx = 0, OCTH(1:0) = 00B. Refer to VREF Unidir.		+3 × VDD / 10		V
	$V_{OCTH2\ Unidir}$	CSDx = 0, OCTH(1:0) = 01B. Refer to VREF Unidir.		+4 × VDD / 10		V
OC Threshold (CSIP-CSIN), Unidirectional	$V_{OCTH3\ Unidir}$	CSDx = 0, OCTH(1:0) = 10B. Refer to VREF Unidir.		+5 × VDD / 10		V
	$V_{OCTH4\ Unidir}$	CSDx = 0, OCTH(1:0) = 11B. Refer to VREF Unidir.		+6 × VDD / 10		V
High OC Threshold (CSIP-CSIN), Bidirectional	$V_{OCTH1\ BidirH}$	CSDx = 1, OCTH(1:0) = 00B. Refer to VREF Unidir.		+2 × VDD / 20		V
High OC Threshold (CSIP-CSIN), Bidirectional	$V_{OCTH2\ BidirH}$	CSDx = 1, OCTH(1:0) = 01B. Refer to VREF Unidir.		+4 × VDD / 20		V
	$V_{OCTH3\ BidirH}$	CSDx = 1, OCTH(1:0) = 10B. Refer to VREF Unidir.		+5 × VDD / 20		V
	$V_{OCTH4\ BidirH}$	CSDx = 1, OCTH(1:0) = 11B. Refer to VREF Unidir.		+6 × VDD / 20		V
Low OC Threshold (CSIP-CSIN), Bidirectional	$V_{OCTH1\ BidirL}$	CSDx = 1, OCTH(1:0) = 00B. Refer to VREF Unidir.		–2 × VDD / 20		V
	$V_{OCTH2\ BidirL}$	CSDx = 1, OCTH(1:0) = 01B. Refer to VREF Unidir.		–4 × VDD / 20		V
	$V_{OCTH3\ BidirL}$	CSDx = 1, OCTH(1:0) = 10B. Refer to VREF Unidir.		–5 × VDD / 20		V
	$V_{OCTH4\ BidirL}$	CSDx = 1, OCTH(1:0) = 11B. Refer to VREF Unidir.		–6 × VDD / 20		V
THERMAL WARNING AND SHUTDOWN						
Thermal Warning Junction Temperature	T_{jW}		120	140	160	°C
Thermal Shutdown Junction Temperature	T_{jSD}		160	180	200	°C
Thermal Shutdown Hysteresis	T_{jHYS}			10		°C
Ratio of T_{jSD} to T_{jW}	T_{jSD} / T_{jW}			1.2		
Thermal Warning Filter Time	t_{jW_FILT}		7	10	13	µs
Thermal Shutdown Filter Time	t_{jSD_FILT}		7	10	13	µs

Note 1: Not subject to production test, specified by design.

Note 2: t_{FOC} refers to the output of the current sense amplifier. The CSO settling time (2µs max, t_{SET}) and the analog propagation delay (< 1µs) are not taken into account by the overcurrent filter time.

5.5.6 SPI INTERFACE

Table 13 lists the electrical characteristics (SPI interface) of DR7808Q . VM = 6.0V to 18V if VSOVTH = 0, VM = 6.0V to 28V if VSOVTH = 1; V_{DD} = 3.0V to 5.5V, T_J = –40°C to 150°C, all voltages with respect to ground. Positive current flowing into pin, unless otherwise specified.

Table 13. Electrical Characteristics (SPI Interface)

PARAMETER	SYMBOL	MIN	NOM	MAX	UNITS
Minimum SPI Clock Period	$t_{(CLK)}$	100			ns
Clock High Time	$t_{(CLKH)}$	40			ns
Clock Low Time	$t_{(CLKL)}$	40			ns
SDI Input Data Setup Time	$t_{(SU\_SDI)}$	20			ns
SDI Input Data Hold Time	$t_{(HD\_SDI)}$	30			ns
SDO Output Hold Time	$t_{(HD\_SDO)}$	50			ns
CSN Setup Time	$t_{(SU\_CSN)}$	50			ns
CSN Hold Time	$t_{(HD\_CSN)}$	50			ns
CSN Minimum High Time Before SCS Active Low	$t_{(HI\_CSN)}$	400			ns
SPI Read After Power On	$t_{(SPI\_READY)}$			10	ms
SDO Output Data Delay Time, CLK High to SDO Valid	$t_{d(SDO)}$		50		ns
SCS Access Time, CSN Low to SDO Out of High Impedance	t_a		100		ns
CSN Disable Time, CSN High to SDO High Impedance	t_{dis}		50		ns

Note 1: Not subject to production test, specified by design.

Note 2: Delay required between EN rising edge and the moment when the device can accept SPI commands.

6. TYPICAL CHARACTERISTICS

TBD

7. 详细说明

7.1 概述

DR7808Q 是一款多通道智能半桥驱动器，集成有八个半桥，其最多可以驱动 16 个外部 NMOSFET。DR7808Q 通常用于直流电机驱动控制，典型应用包括汽车电动座椅控制，车门控制等。

DR7808Q 支持 24 位 SPI，可以实现芯片功能配置，状态检测诊断，甚至可以控制半桥。SPI 读取状态寄存器可以实现例如电源电压监控、电荷泵电压、温度警告和过温关断等诊断。每个栅极驱动器监控独立于其外部 MOSFET 漏极-源极电压以应对故障情况。

除了 SPI, DR7808Q 还可以通过 PWM1/2/3 三个输入 IO 进行半桥控制。该器件采用 QFN-48 封装，下方带有散热焊盘，可供良好的热性能并最大限度地减少所需的 PCB 空间。

7.2 功能模块框图

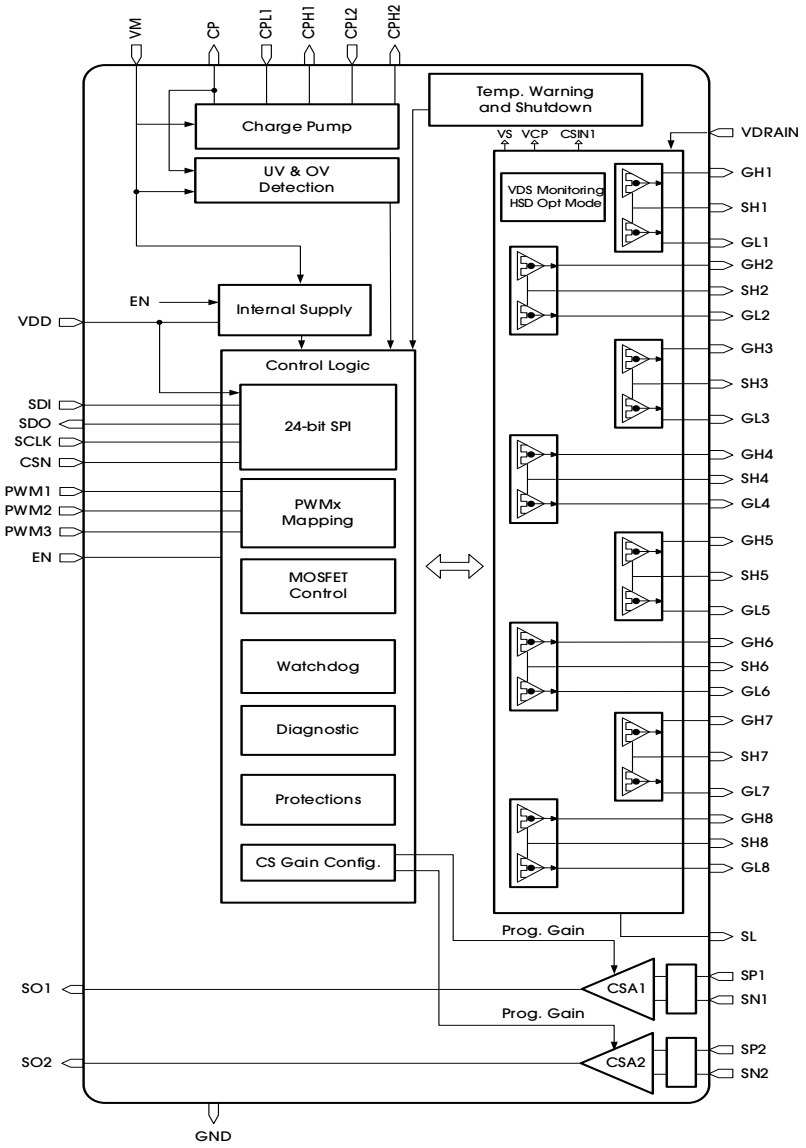


Figure 2. Functional Block Diagram

7.3 电源供电

DR7808Q 有两组电源，V_S 和 V_{DD}。V_{DD} 主要给所有数字 IO 和内部的逻辑电路供电，其可以支持 3.3V 或者 5.0V 电平。V_S 为电荷泵供电，可以实现 MOSFET 的栅极驱动控制。V_S 一般是通过电池反接电路直接连接到汽车电池上。

V_S 和 V_{DD} 是两组独立的电源，如果 V_S 掉电而 V_{DD} 未掉电，则所有配置信息可以得到保留。反之，不管 V_S 是否掉电，只要 V_{DD} 掉电，所有的配置信息都会被重置。在上电时序方面，DR7808Q 这两组电源没有先后之分。建议电路设计中在靠近 pin 脚附近增加 0.1uF 的贴片陶瓷去耦电容。

7.4 RESET 行为

触发 POR(Power On Reset)的事件包括：

V_{DD} **欠压复位**:

如果 $V_{DD} < V_{DD\ PoffR}$，输出都会关闭，内部数字模块处于关闭状态。一旦 $V_{DD} > V_{DD\ POR}$，内部数字模块将会复位， NPOR (negated power-on reset, global status byte)位会被复位为 0 来报告复位。

EN **复位引脚**:

如果 EN 引脚被拉低，芯片内部的逻辑将会被复位，并且芯片进入睡眠模式（sleep mode）。此时如果芯片重新进入正常模式（Normal Mode，需要 EN 为高,持续 t_{SET_SPI} 且 $V_{DD} > V_{DD\ POR}$），NPOR (negated power-on reset, global status byte)位会被复位为 0 来报告复位。

当 GENSTAT 被清零时，NPOR 为被置 1.

7.5 工作模式

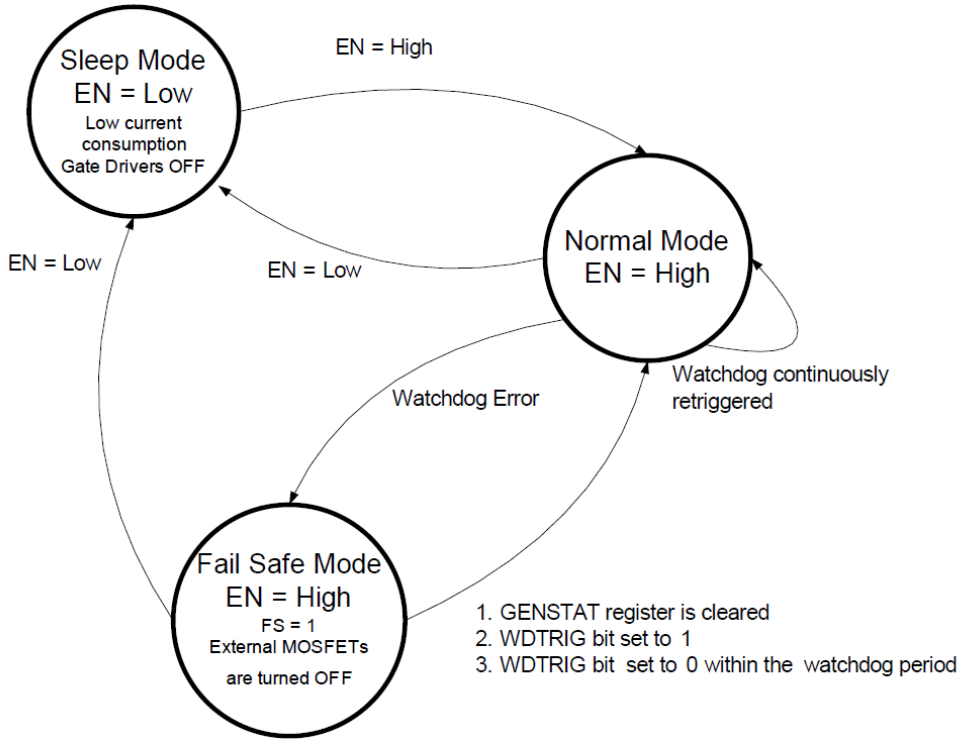


Fig 工作状态机

请注意，上述状态机是在 Vs, VDD 供电正常的情况。

7.5.1 Normal 模式

DR7808Q 进入 Normal 模式条件为:置高 EN 并且持续 SPI setup 时间 t_{SET_SPI}. 在 normal 模式下，如果电源供电正常，输出栅极驱动器会被使能，并且可以通过 SPI 进行配置控制。为了保持在 normal 模式下， 看门狗必须被正确地重置。

7.5.2 Sleep 模式

DR7808Q 进入 Sleep 模式条件为:置低 EN 并且持续 t_{DSLEEP} （max tCCP of active half-bridges + 3us)。该时间主要为了外部 MOS 有足够时间被关断。在 Sleep 模式，内部 LDO 和内部电路都会被关闭，SPI 寄存器会被重置复位。

在芯片 GHx/GLx 和 GND 之间有一个内部电阻 R_{GGND}，其作用为给外部 MOSFETs 的栅极进行放电。

Note:如果 EN 设置为低电平的持续时间短于（tENL_FILT，最长 8μs)，并且 EN 再次设置为高电平，则器件不会进入睡眠模式，寄存器也不会复位。当 EN 为高电平时，半桥根据控制寄存器的设置重新激活。

7.5.3 Fail Safe 模式

如果出现看门狗错误(请参阅第 7.10 章)，器件将进入故障安全模式，设置 FS 位(请参阅全局状态字节)，并且外部 MOSFET 在有效的最大配置 tHBxCCP 期间通过静态放电电流主动放电。然后将桥驱动器设置为 passive 模式（passive 放电路径被激活，第 6.4 章，所有外部 MOSFET 被锁断，并且电荷泵被停用)。要恢复正常模式，MCU 必须执行以下序列 2):

1.清除 GENSTAT 寄存器;

2.在 watchdog 周期内，对 WDTRIG(GENCTRL1)写 1;

3.在 watchdog 周期内，对 WDTRIG(GENCTRL1)写 0 (1);

（1）在 failsafe 模式期间，电荷泵被停用。

在故障安全模式下，控制寄存器被冻结为其默认值，WDTRIG、PASS_VDS、PASS_MOD、CSA1L、CSA2L 除外。在此模式下，任何写命令（WDTRIG 位除外）或清除命令（GENSTAT 除外）都将被丢弃并设置 SPIE 位（全局状态字节)。

在故障安全模式下对 GENSTAT 的清除命令不会重置该状态寄存器报告的任何故障标志。

在退出序列开始之前，可以在此模式下读取控制和状态寄存器，而不会设置 SPIE 位。

7.6 电荷泵

双级电荷泵为高侧和低侧 MOSFET 提供栅极驱动器。它需要在 CPC1N 和 CPC1P、CPC2N 和 CPC2P、VM 和 CP 之间连接三个外部电容器。

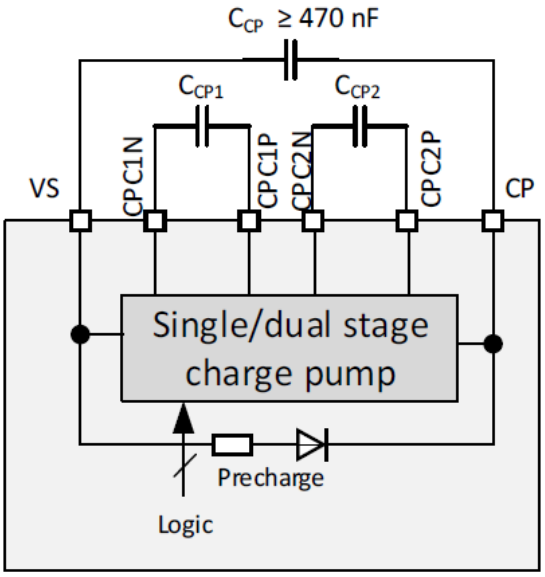


Figure 3. Bridge Control

如果 CPSTGA=1(GENCTRL2)，芯片会自动切换到单级或双级电荷泵：

- 如果 VM > VCPSO DS：DR7808Q 从双级电荷泵切换为单级电荷泵。
- 如果 VM < VCPSO SD：DR7808Q 从单级电荷泵切换到双级电荷泵。

单级电荷泵的运行降低了 VM 引脚的电流消耗。

7.6.1 电荷泵频率调制

可以激活电荷泵频率的调制以减少峰值发射。 在 EMC 测试期间，可以根据峰值检测器的分辨率带宽来选择调制频率。调制频率由 GENCTRL1 中的控制位 FMODE 设置

- FMODE = 0: 无频率调制.
- FMODE = 1: 调制频率 = 15.6 kHz (默认设置).

7.7 编程控制

7.7.1 SPI 接口

DR7808Q 作为从机，支持主控以 24 位串行外设接口(SPI)进行通信。主控可以通过 SPI 对芯片进行配置和控制，并读取状态寄存器以实现诊断。

该接口包括：

- 数据输入引脚(SDI)，用于将数据传输到从机；
- 数据输出引脚(SDO)，用于从从设备读回数据；
- 串行时钟引脚(SCLK)，用于数据输入和输出时钟。
- 片选引脚(CSN)启用或禁用串行接口。

SPI 帧从 CSN 的下降沿开始。在 CSN 的下降沿期间，SCLK 必须为低电平（时钟极性 CPOL=0)。SDI 上接收到的数据在 SCLK 的下降沿移入。通过 SDO 传输数据在 SCLK 的上升沿移出（时钟相位 CPHA=1)。

输出传输时，最高有效位（MSB，位 23）首先移入/移出。写入和清除命令在 CSN 的上升沿执行。SPI 协议支持独立从机选择和菊花链配置。

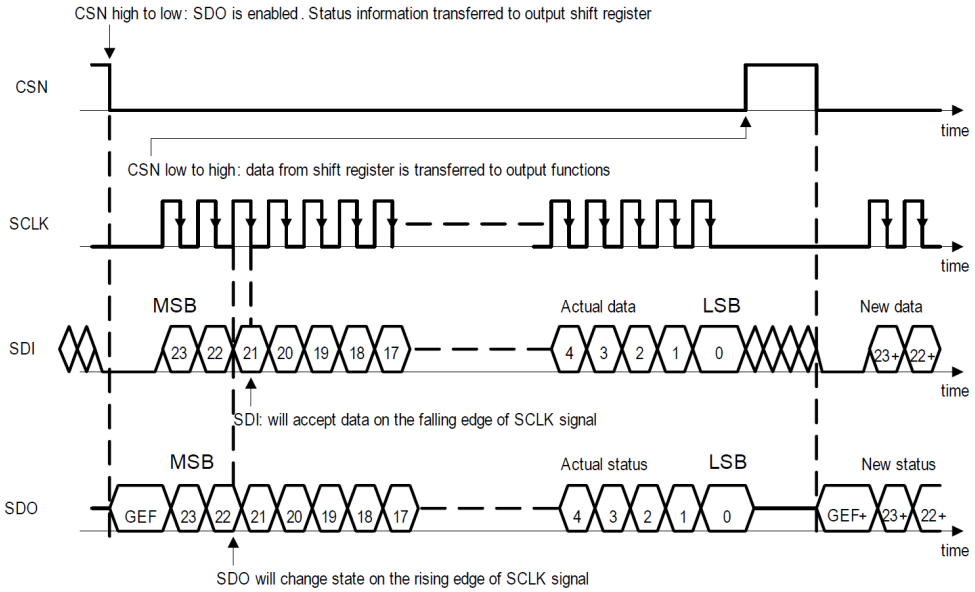
7.7.2 SPI 帧格式

7.7.2.1 FRAME

SPI 通信由 24 位帧组成

•SDI 接收一个地址字节，其后为两个数据字节。

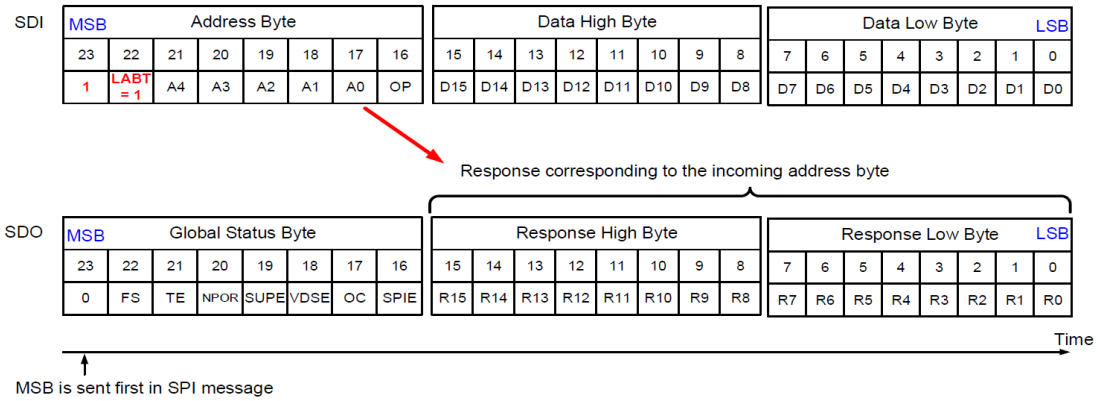
•SDO 传输全局错误标志和全局状态字节，后跟两个响应字节



请注意：地址字节的 MSB 必须设置为 “1”。

- 地址字节指定（参见下图）：
- 目标寄存器（A(4:0)）
- 操作类型：
- 对于控制寄存器：
  - 只读：OP 位 1) = ‘0’
  - 读取和写入：OP 位 = ‘1’
- 对于状态寄存器：
  - 只读：OP 位 = ‘0’
  - 读取并清除：OP 位 = ‘1’

请注意，对于单独的从机，最后地址字节令牌(LABT)必须设置为 “1” 。



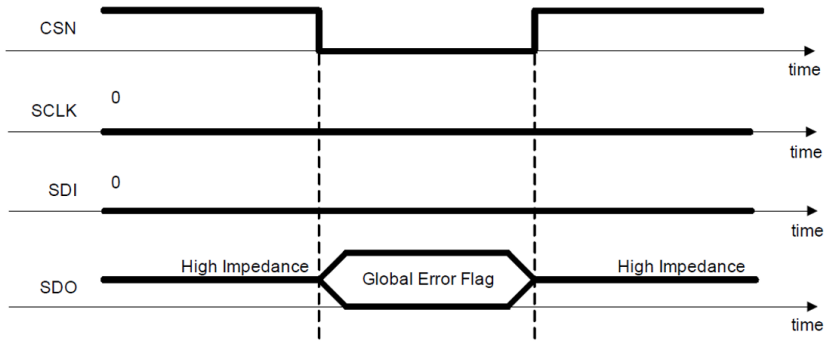
7.7.2.2 IN-FRAME RESPONSE

SPI 协议包含帧内响应：寻址寄存器的内容由同一 SPI 帧内的 SDO 移出。此功能可减少读取控制或状态寄存器期间的 SPI 总线负载。具体如上图所示，SDO 可以同步给出 Global Status Byte 并附加 SDI 对应寄存器地址的数据。

7.7.3 Global Error Flag (GEF)

Global Error Flag (GEF)在 CSN 下降沿和第一个 SCLK 上升沿之间的 SDO 上报告。如果检测到故障情况或设备来自上电复位(POR)，则设置 GEF。因此是无需任何 SPI 时钟脉冲即可进行快速设备诊断。

针对此应用，需要特殊时序，请联系类比技术支持。



7.7.4 Global status byte

SDO 在前 8 个 SCLK 周期内移出全局状态字节（Global Status Byte）。该寄存器提供了设备状态的概述并可以报告如下错误情况:、

- 故障保护（FS 位）。
- 温度错误（TE 位）：热警告（TW）和热之间的逻辑或组合关闭（TSD）。
- 取反上电复位（NPOR 位）。
- 电源错误（SUPE 位）：VM 欠压关断(VSUV)、VM 之间的逻辑或组合过压关断（VSOV)和电荷泵欠压(CPUV)。
- VDS 监控错误（VDSE 位）：DSOV 寄存器的位之间的逻辑或组合。
- 过流（OC 位）：OC1 和 OC2 状态位（GENSTAT 寄存器）之间的逻辑或组合。
- SPI 协议错误（SPIE 位）。

备注：全局错误标志是全局状态字节和 TDREGx 的每一位的逻辑或的组合：

GEF=(FS) 或 (TE) 或 (NOT(NPOR)) 或 (SUPE) 或 (VDSE) 或 (OC) 或 (SPIE) 或 (NOT(TDREGx) AND (PWMx_EN =1) 与（非 (MSKTDREG)))，x = 1 ... 3。

下表显示了如何在全局状态字节和错误标志中报告故障：

Table 26 Failure reported in the global status byte and global error flag

Type of Error	Failure reported in the Global Status Byte	Global Error Flag
Fail safe	FS = 1	1
Thermal error	TE = 1	1
Power ON reset	NPOR = 0	1
Supply error	SUPE = 1	1
Drain source voltage monitoring	VDSE = 1	1
Overcurrent	OC = 1	1
SPI protocol error	SPIE = 1	1
TDREGx, x = 1 ... 31) (see GENSTAT)	-	1 if MSKTDREG = 02) 0 if MSKTDREG = 12)
No error and no power ON reset	SPIE = 0 OC = 0 VDSE = 0 SUPE= 0 NPOR = 1 TE = 0 FS = 0	0

	TDREGx = 0,	

1) See status register **GENSTAT.**

2) See control register **GENCTRL2**.

注：NPOR 的默认值（上电复位后）为 0，因此 GEF 的默认值为 1。在故障安全模式下，控制寄存器被冻结为其默认值，WDTRIG 位除外。故障安全模式下的任何写访问（WDTRIG 位除外）都将被丢弃，并且 SPIE 位将被置位。

7.7.5 SPI Error Detection

SPI 在全局状态字节(SPIE)中包含一个错误标志，以监督和保持数据完整性。如果在给定帧期间检测到 SPI 协议错误，则在下一个 SPI 通信中设置 SPIE 位。SPIE 位在以下错误条件下被置位：

- CSN 为低电平时接收到的 SCLK 时钟脉冲数为（协议错误）：
  - 不为零
  - 或小于 24
  - 或超过 24 但不是 8 的倍数
- 微控制器向未使用的地址发送 SPI 命令（协议错误）。
- 检测到时钟极性错误：输入时钟信号为高电平
- 在 CSN 上升沿或下降沿期间（协议错误）。
- 未检测到地址字节或未检测到最后一个地址字节（协议错误）。
- 在菊花链中：微控制器不会按顺序发送第一个地址字节，直到最后一个地址字节（即两个地址字节之间有间隙）。 在这种情况下，SDO 信号在 SPI 帧的剩余部分被设置为 ‘0’ 1)，以防止其他设备执行错误的命令（协议错误）。
- 地址 0x1F（设备 ID 寄存器，偏移地址= 0x1F）的清除命令。
- 相同的半桥被分配给多个激活的 PWM 通道。
- 在故障安全模式下接收到的任何写入或清除命令，且不属于退出序列。

注：激活映射到多个 PWM 通道的半桥的 SPI 命令将被忽略。在故障安全模式下，除了写入 WDTRIG 之外，不能访问控制寄存器。无效写入该模式下的命令设置 SPIE 位。

正确的 SPI 通信：

•在 CSN 下降沿之前 SCLK 必须保持低电平至少 tBEF，在 CSN 下降沿之后保持低电平 tlead。

•SCLK 必须在 CSN 上升沿之前为低电平并保持最小延迟，在 CSN 上升沿之后为 tBEH。

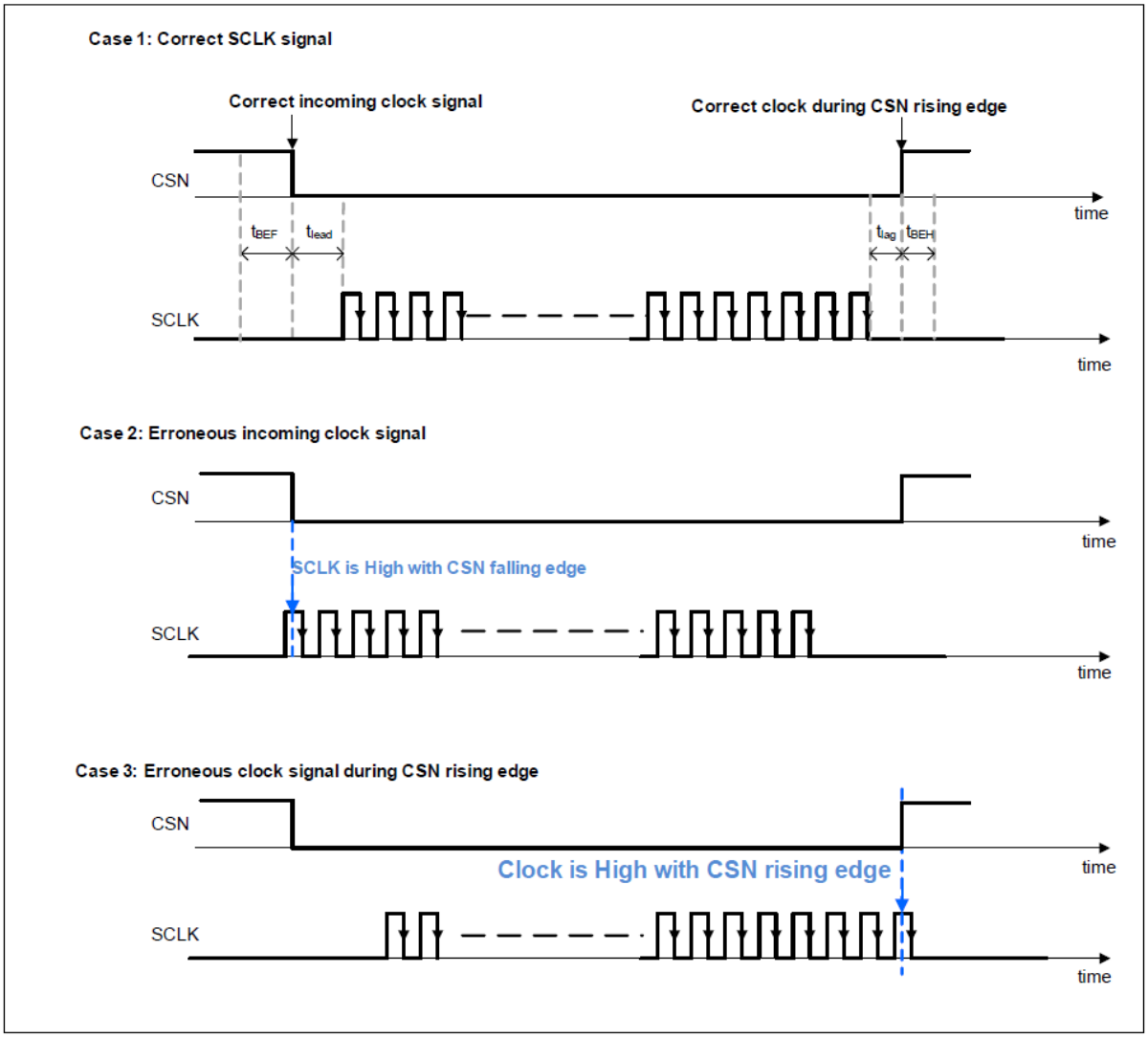


Figure 45 Clock polarity error

SPIE 位的复位条件取决于错误原因：

- 在正常模式下：
  - 如果一个半桥已分配给多个半桥，则微控制器必须清除 HBVOUT_PWMERR。
  - 对于 SPIE 报告的其他错误，微控制器必须发送正确的 SPI 帧。
- 如果 SPIE 已设置为故障安全模式，则器件必须首先进入正常模式。

8. REGISTER MAPS

8.1 CONTROL REGISTERS

Table 14. Register Overview

REGISTER SHORT NAME	REGISTER LONG NAME	OFFSET ADDRESS	RESET VALUE
GENCTRL1	General control register 1	0x00 and REG_BANK = 0 or 1	0x0026
GENCTRL2	General control register 2	0x01 and REG_BANK = 0 or 1	0x4180
VDS1	Drain-source monitoring HB1-4	0x02 and REG_BANK = 0 or 1	0x0249
VDS2	Drain-source monitoring HB5-8	0x03 and REG_BANK = 0 or 1	0x0249
CCP_BLK1	Cross current protection and blank times setting 1	0x04 and REG_BANK = 0 or 1	0x0000
CCP_BLK2_ACT	Cross current protection and blank times setting for active MOSFETs (1)	0x05 and REG_BANK = 0	0x4924
CCP_BLK2_FW	Cross current protection and blank times setting for FW MOSFETs (1)	0x05 and REG_BANK = 1	0x4924
HBMODE	Half-bridge mode	0x06 and REG_BANK = 0 or 1	0x0000
PWMSET	Setting of PWM channels	0x07 and REG_BANK = 0 or 1	0x6C60
TPRECHG	PWM pre-charge and pre-discharge time	0x08 and REG_BANK = 0 or 1	0x0000
HBIDIAG	Half-bridge diagnostic current control	0x09 and REG_BANK = 0 or 1	0xC000
ST_ICHG	Charge current for static half-bridges	0x0A and REG_BANK = 0	0x0044
PWM_PCHG_INIT	Precharge current initialization	0x0A and REG_BANK = 1	0x18C6
PWM_ICHG_ACT	Charge current for half-bridges in PWM (active MOSFETs)	0x0B and REG_BANK = 0	0x18C6
PWM_ICHG_FW	Charge current for half-bridges in PWM (FW MOSFETs)	0x0B and REG_BANK = 1	0x18C6
PWM_IDCHG_ACT	Discharge current of active MOSFETs in PWM operation	0x0C and REG_BANK = 0	0x1CE7
PWM_PDCHG_INIT	Predischarge current initialization	0x0C and REG_BANK = 1	0x318C
PWM_ICHGMAX_CCP_BLK3_ACT	Max. pre-charge / pre-discharge currents for half-bridges in PWM(1), t_{CCP} and t_{BLANK} setting for active MOSFETS	0x0D and REG_BANK =0	0x4900
PWM_ICHGMAX_CCP_BLK3_FW	Max. pre-charge / pre-discharge currents for half-bridges in PWM(1), t_{CCP} and t_{BLANK} setting for FW MOSFETS TDON_OFF3	0x0D and REG_BANK =1	0x4900
TDON_OFF1	Turn-on and turn-off delays for PWM channel1	0x0E and REG_BANK = 0 or 1	0x0A0A
TDON_OFF2	Turn-on and turn-off delays for PWM channel2	0x0F and REG_BANK = 0 or 1	0x0A0A
TDON_OFF3	Turn-on and turn-off delays for PWM channel3	0x10 and REG_BANK = 0 or 1	0x0A0A
DRV_LPWR_EN	Half bridges drv low power mode enable and high hardoff current enable	0x1C and REG_BANK = 0 or 1	0x0200
CSA_OC_SH	Half bridges OC and SH configuration for Current sense amplifier 1 and Current sense amplifier 2	0x1D and REG_BANK = 0 or 1	0x0000
MISC	Miscellaneous functions configuration	0x1E and REG_BANK = 0 or 1	0x0000

Note: ICHGMAX is also the current applied to the Active MOSFET during post-discharge.

8.2 GENERAL CONTROL REGISTERS AND PROTECTION SETTINGS

8.2.1 GENERAL CONTROL REGISTER 1

General Control Register 1 (0 0000B) Reset Value: 0000 0000 0010 0110B

Table 15. General Control Register 1

BIT	FIELD	TYPE	DESCRIPTION
15	CSD2	R/W	Direction of the current sense amplifier 2 0B: The current sense is unidirectional (default). 1B: The current sense is bidirectional.
14:13	CSAG2	R/W	Gain of the current sense amplifier 2 00B: 10V/V default 01B: 20V/V 10B: 40V/V 11B: 80V/V
12	CSD1	R/W	Direction of the current sense amplifier 1 0B: The current sense is unidirectional (default). 1B: The current sense is bidirectional.
11:10	CSAG1	R/W	Gain of the current sense amplifier 1 00B: 10V/V (default) 01B: 20V/V 10B: 40V/V 11B: 80V/V
9	REG_BANK	R/W	Register banking 0B (default): Refer to CCP_BLK2_ACT, PWM_ICHGMAX_CCP_BLK3_ACT, PWM_ICHG_ACT, ST_ICHG, and PWM_IDCHG_ACT. 1B: Refer to CCP_BLK2_FW, PWM_ICHGMAX_CCP_BLK3_FW, PWM_ICHG_FW, PWM_PDCHG_INIT, and PWM_PCHG_INIT
8	VSOVTH	R/W	VM overvoltage threshold 0B: VSOV OFF = VSOV OFF1 (min. 19V, default) 1B: VSOV OFF = VSOV OFF2 (min. 29V)
7	UNLOCK	R/W	Unlock bit to disable the watchdog 0B: WDDIS cannot be reset (default). 1B: WDDIS (GENCTRL2) can be reset in the following SPI frame.
6	Reserved	R	Reserved. Always read as '0'
5	FMODE	R/W	Frequency modulation 0B: No modulation 1B: Modulation frequency 15.6 kHz (default)
4	Reserved	R	Reserved. Always read as '0'
3	IPCHGADT	R/W	Adaptation of the pre-charge and pre-discharge current 0B: 1 current step (default) 1B: 2 current steps
2	OCEN	R/W	Overcurrent shutdown enable 0B: Disable 1B: Enabled (default)
1	WDPER	R/W	Watchdog period 0B: 50ms 1B: 200ms (default)
0	WDTRIG	R/W	Watchdog trigger bit This bit must be inverted within a watchdog period. After power-on reset, the default value is 0.

8.2.2 GENERAL CONTROL REGISTER 2

GENCTRL2 General Control Register 2 (0 0001B:) Reset Value: 0100 0001 1000 0000B:

Table 16. General Control Register 2

BIT	FIELD	TYPE	DESCRIPTION
15	POCHGDIS	R/W	Postcharge disable bit 0B: The postcharge phase is enabled during PWM (default). 1B: The postcharge phase is disabled during PWM.
14	BD_PASS	R/W	Bridge driver passive mode 0B: Bridge driver is in active mode. 1B: Bridge driver is in passive mode (Default).
13	AGCFILT	R/W	Filter for adaptive gate control Refer to adaptive control of pre-charge current and adaptive control of pre-discharge current. 0B: No filter applied (default) 1B: Filter applied
12:11	AGC	R/W	Adaptive gate control 00B: Adaptive gate control disabled, pre-charge and pre-discharge disabled (default) 01B: Adaptive gate control disabled, pre-charge disabled. Pre-discharge is enabled with IPREDCHG = IPDCHGINIT (refer to PWM_PCHG_INIT.) 10B: Adaptive gate control enabled, and IPRECHG and IPREDCHG self-adapted 11B: Reserved. Adaptive gate control enabled, and IPRECHG and IPREDCHG are self adapted
10	IHOLD	R/W	Gate driver hold current IHOLD 0B (default): Charge: ICHG8 (12.5mA typ.), discharge IDCHG8 (14.2mA typ.) 1B: Charge: ICHG12 (23.9mA typ.), discharge: IDCHG12 (26.0mA typ.)
9	WDDIS	R/W	Watchdog disable bit 0B: The watchdog is enabled (default). 1B: The watchdog is disabled if the previous SPI frame has set the UNLOCK bit (GENCTRL1). Once the watchdog is disabled, it is directly re-enabled by resetting WDDIS.
8	MSKTDREG	R/W	Masking of the turn-on/-off delay error in the Global Error Flag (GEF) 0B: Turn-on/-off delay error is reported in the GEF. 1B: Turn-on/-off delay error is masked in the GEF (default).
7	CPUVTH	R/W	Charge pump undervoltage detection threshold 0B: VCPUV (referred to VM) = 6.0V typ. 1B: VCPUV (referred to VM)= 7.5V typ. (default)
6	CPSTGA	R/W	Automatic switch-over between dual and single charge pump stage 0B: Automatic switch-over deactivated (default) 1B: Automatic switch-over activated
5:4	TFVDS	R/W	Filter time of drain-source voltage monitoring 00B: 0.5µs (default) 01B: 1µs 10B: 2µs 11B: 3µs
3:2	OCTH2	R/W	Overcurrent detection threshold of SO2 with CSD2 = 0 00B: VSO2 > VDD / 2 (default) 01B: VSO2 > VDD / 2 + VDD / 10 10B: VSO2 > VDD / 2 + 2 x VDD / 10 11B: VSO2 > VDD / 2 + 3 x VDD / 10 Overcurrent detection threshold of SO2 with CSD2 = 1 00B: VSO2 > VDD / 2 + 2 x VDD / 20 or VSO2 < VDD / 2 – 2 x VDD / 20 (default) 01B: VSO2 > VDD / 2+ 4 x VDD / 20 or VSO2 < VDD / 2 – 4 x VDD / 20

BIT	FIELD	TYPE	DESCRIPTION
			10B: VSO2 > VDD / 2+ 5 x VDD / 20 or VSO2 < VDD / 2 – 5 x VDD / 20 11B: VSO2 > VDD / 2+ 6 x VDD / 20 or VSO2 < VDD / 2 – 6 x VDD / 20
1:0	OCTH1	R/W	Overcurrent detection threshold of SO1 with CSD1 = 0 00B: VSO1 > VDD / 2 (default) 01B: VSO1 > VDD / 2 + VDD / 10 10B: VSO1 > VDD / 2 + 2 x VDD / 10 11B: VSO1 > VDD / 2 + 3x VDD / 10 Overcurrent detection threshold of SO1 with CSD1 = 1 00B: VSO1 > VDD / 2+2 x VDD / 20 or VCSOx < VDD / 2 – 2 × VDD / 20 (default) 01B: VSO1 > VDD / 2+ 4x VDD / 20 or VCSOx < VDD / 2 – 4 × VDD / 20 10B: VSO1 > VDD / 2+ 5 x VDD / 20 or VCSOx < VDD / 2 – 5 × VDD / 20 11B: VSO1 > VDD / 2+ 6x VDD / 20 or VCSOx < VDD / 2 – 6 × VDD / 20

8.2.3 DRAIN-SOURCE MONITORING HB1-4

VDS1 Drain-source monitoring threshold HB1-4 (0 0010_B:)Reset Value:0000 0010 0100 1001B:

Table 17. Drain-Source Monitoring Threshold HB1-4

BIT	FIELD	TYPE	DESCRIPTION
15	HB4D	R/W	Reserved
14	HB3D	R/W	Reserved
13	HB2D	R/W	Reserved
12	HB1D	R/W	Reserved
11:9	HB4VDSTH	R/W	HB4 drain-source overvoltage threshold 000B: 0.15V 001B: 0.20V (default) 010B: 0.25V 011B: 0.30V 100B: 0.40V 101B: 0.50V 110B: 0.60V 111B: 2.0V
8:6	HB3VDSTH	R/W	HB3 drain-source overvoltage threshold 000B: 0.15V 001B: 0.20V (default) 010B: 0.25V 011B: 0.30V 100B: 0.40V 101B: 0.50V 110B: 0.60V 111B: 2.0V
5:3	HB2VDSTH	R/W	HB2 drain-source overvoltage threshold 000B: 0.15V 001B: 0.20V (default) 010B: 0.25V 011B: 0.30V 100B: 0.40V 101B: 0.50V 110B: 0.60V 111B: 2.0V
2:0	HB1VDSTH	R/W	HB1 drain-source overvoltage threshold 000B: 0.15V 001B: 0.20V (default) 010B: 0.25V 011B: 0.30V 100B: 0.40V

			101B: 0.50V 110B: 0.60V 111B: 2.0V

8.2.4 DRAIN-SOURCE MONITORING HB5-8

VDS2 Drain-source monitoring threshold HB5-8 (0 0011B:) Reset Value: 0000 0010 0100 1001B:

Table 18. Drain-Source Monitoring Threshold HB5-8

BIT	FIELD	TYPE	DESCRIPTION
15	HB8D	R/W	Reserved
14	HB7D	R/W	Reserved
13	HB6D	R/W	Reserved
12	HB5D	R/W	Reserved
11:9	HB8VDSTH	R/W	HB8 drain-source overvoltage threshold 000B: 0.15V 001B: 0.20V (default) 010B: 0.25V 011B: 0.30V 100B: 0.40V 101B: 0.50V 110B: 0.60V 111B: 2.0V
8:6	HB7VDSTH	R/W	HB7 drain-source overvoltage threshold 000B: 0.15V 001B: 0.20V (default) 010B: 0.25V 011B: 0.30V 100B: 0.40V 101B: 0.50V 110B: 0.60V 111B: 2.0V
5:3	HB6VDSTH	R/W	HB6 drain-source overvoltage threshold 000B: 0.15V 001B: 0.20V (default) 010B: 0.25V 011B: 0.30V 100B: 0.40V 101B: 0.50V 110B: 0.60V 111B: 2.0V
2:0	HB5VDSTH	R/W	HB5 drain-source overvoltage threshold 000B: 0.15V 001B: 0.20V (default) 010B: 0.25V 011B: 0.30V 100B: 0.40V 101B: 0.50V 110B: 0.60V 111B: 2.0V

8.2.5 CROSS CURRENT PROTECTION AND BLANK TIMES SETTING 1

CCP_BLK1 CCP and Blank times setting 1 (0 0100B:)Reset Value: 0000 0000 0000 0000B:

Table 19. CCP and Blank Times Setting 1

BIT	FIELD	TYPE	DESCRIPTION
15:14	HB8CCPBLK	R/W	Cross-current protection and blank times applied to HB8 00B: (tHB8CCP, tHB8B: LANK) = (tCCP1, tBLANK1) (default) 01B: (tHB8CCP, tHB8B: LANK) = (tCCP2, tBLANK2) 10B: (tHB8CCP, tHB8B: LANK) = (tCCP3, tBLANK3) 11B: (tHB8CCP, tHB8B: LANK) = (tCCP4, tBLANK4)
13:12	HB7CCPBLK	R/W	Cross-current protection and blank times applied to HB7 00B: (tHB7CCP, tHB7B: LANK) = (tCCP1, tBLANK1) (default) 01B: (tHB7CCP, tHB7B: LANK) = (tCCP2, tBLANK2) 10B: (tHB7CCP, tHB7B: LANK) = (tCCP3, tBLANK3) 11B: (tHB7CCP, tHB7B: LANK) = (tCCP4, tBLANK4)
11:10	HB6CCPBLK	R/W	Cross-current protection and blank times applied to HB6 00B: (tHB6CCP, tHB6B: LANK) = (tCCP1, tBLANK1) (default) 01B: (tHB6CCP, tHB6B: LANK) = (tCCP2, tBLANK2) 10B: (tHB6CCP, tHB6B: LANK) = (tCCP3, tBLANK3) 11B: (tHB6CCP, tHB6B: LANK) = (tCCP4, tBLANK4)
9:8	HB5CCPBLK	R/W	Cross-current protection and blank times applied to HB5 00B: (tHB5CCP, tHB5B: LANK) = (tCCP1, tBLANK1) (default) 01B: (tHB5CCP, tHB5B: LANK) = (tCCP2, tBLANK2) 10B: (tHB5CCP, tHB5B: LANK) = (tCCP3, tBLANK3) 11B: (tHB5CCP, tHB5B: LANK) = (tCCP4, tBLANK4)
7:6	HB4CCPBLK	R/W	Cross-current protection and blank times applied to HB4 00B: (tHB4CCP, tHB4B: LANK) = (tCCP1, tBLANK1) (default) 01B: (tHB4CCP, tHB4B: LANK) = (tCCP2, tBLANK2) 10B: (tHB4CCP, tHB4B: LANK) = (tCCP3, tBLANK3) 11B: (tHB4CCP, tHB4B: LANK) = (tCCP4, tBLANK4)
5:4	HB3CCPBLK	R/W	Cross-current protection and blank times applied to HB3 00B: (tHB3CCP, tHB3B: LANK) = (tCCP1, tBLANK1) (default) 01B: (tHB3CCP, tHB3B: LANK) = (tCCP2, tBLANK2) 10B: (tHB3CCP, tHB3B: LANK) = (tCCP3, tBLANK3) 11B: (tHB3CCP, tHB3B: LANK) = (tCCP4, tBLANK4)
3:2	HB2CCPBLK	R/W	Cross-current protection and blank times applied to HB2 00B: (tHB2CCP, tHB2B: LANK) = (tCCP1, tBLANK1) (default) 01B: (tHB2CCP, tHB2B: LANK) = (tCCP2, tBLANK2) 10B: (tHB2CCP, tHB2B: LANK) = (tCCP3, tBLANK3) 11B: (tHB2CCP, tHB2B: LANK) = (tCCP4, tBLANK4)
1:0	HB1CCPBLK	R/W	Cross-current protection and blank times applied to HB1 00B: (tHB1CCP, tHB1B: LANK) = (tCCP1, tBLANK1) (default) 01B: (tHB1CCP, tHB1B: LANK) = (tCCP2, tBLANK2) 10B: (tHB1CCP, tHB1B: LANK) = (tCCP3, tBLANK3) 11B: (tHB1CCP, tHB1B: LANK) = (tCCP4, tBLANK4)

8.2.6 CROSS CURRENT PROTECTION AND BLANK TIMES SETTING FOR ACTIVE MOSFETS1

CCP_BLK2_ACT Active CCP and Blank times setting 2 (0 0101B:)Reset Value: 0100 1001 0010 0100B:

BIT	FIELD	TYPE	DESCRIPTION
15	Reserved	R	Reserved. Always read as '0'.
14:12	TCCP3_ACT	R/W	Cross-current protection - tCCP3 Active Refer to Table 29 100B (default): 2000ns typ.
11:9	TBLANK2_A CT	R/W	Blank time - tBLANK2 Active Refer to Table 30 100B (default): 2000ns typ.
8:6	TCCP2_ACT	R/W	Cross-current protection - tCCP2 Active Refer to Table 29 100B (default): 2000ns typ.
5:3	TBLANK1_A CT	R/W	Blank time - tBLANK1 Active Refer to Table 30 100B (default): 2000ns typ.
2:0	TCCP1_ACT	R/W	Cross-current protection - tCCP1 Active Refer to Table 29 100B (default): 2000ns typ.

Table 20. Cross-Current Protection Time for Active MOSFETs

TCCPX_ACT(2:0), X = 1…4	ACTIVE CROSS-CURRENT PROTECTION HBX, X = 1…4 (TYPICAL)
000B	375ns
001B	625ns
010	1μs
011	1.5μs
100	2μs (default)
101	3μs
110	4μs
111	16μs

Table 21. Drain-Source Overvoltage Blank Time for Active MOSFETs

TBLANKX_ACT(2:0), X = 1…4	ACTIVE DRAIN-SOURCE OVERVOLTAGE BLANK TIME TBLANKX, X = 1…4 (TYPICAL)
000B	625ns
001B	1μs
010B	1.25μs
011B	1.5μs
100B	2μs (default)
101B	3μs
110B	4μs
111B	8us

8.2.7 CROSS CURRENT PROTECTION AND BLANK TIMES SETTING FOR FW MOSFETS1

CCP_BLK2_FW FW CCP and Blank times setting 2 (0 0101B:)Reset Value: 0100 1001 0010 0100B:

Table 22. FW CCP and Blank Times Setting 2

BIT	FIELD	TYPE	DESCRIPTION
15	Reserved	R	Reserved. Always read as '0'.
14:12	TCCP3_FW	R/W	Cross-current protection - tCCP3 freewheeling Refer to Table 31 100B (default): 2000ns typ.
11:9	TBLANK2_F W	R/W	Blank time - tBLANK2 freewheeling Refer to Table 32 100B (default): 2000ns typ.
8:6	TCCP2_FW	R/W	Cross-current protection - tCCP2 freewheeling Refer to Table 31 100B (default): 2000ns typ.
5:3	TBLANK1_F W	R/W	Blank time - tBLANK1 freewheeling Refer to Table 32 100B (default): 2000ns typ.
2:0	TCCP1_FW	R/W	Cross-current protection - tCCP1 freewheeling Refer to Table 31 100B (default): 2000ns typ.

Table 23. Drain-Source Overvoltage Blank Time for FW MOSFETs

TBLANKX_FW(2:0), X = 1…4	FW DRAIN-SOURCE OVERVOLTAGE BLANK TIME TBLANKX, X = 1…4 (TYPICAL)
000B	625ns
001B	1µs
010B	1.25µs
011B	1.5µs
100B	2µs (default)
101B	3µs
110B	4µs
111B	16µs

Note: When applying a drain-source overvoltage blank time of 16µs to a half-bridge, the maximum drive current used for this half-bridge must be set below 30mA to avoid an overheating of the gate driver. Refer to register ST_ICHG for static controlled half-bridges and PWM_ICHG_FW for half-bridges controlled in PWM. Refer to PWM_ICHGMAX_CCP_BLK3_FW for the setting of tBLANK4, tCCP4, and tBLANK3 for the FW MOSFETs. Refer to CCP_BLK1 for the mapping of (tCCPx, tBLANKx) to the half-bridges.

8.2.8 HALF-BRIDGE MODE

HBMODE Half-bridge mode (0 0110B:)Reset Value: 0B:

Table 24. Half-Bridge Mode

BIT	FIELD	TYPE	DESCRIPTION
15:14	HB8MODE	R/W	Half-bridge output 8 mode selection 00B: HB8 is in high impedance (default). 01B: LS8 is ON. 10B: HS8 is ON. 11B: Reserved - HB8 is in high impedance.
13:12	HB7MODE	R/W	Half-bridge output 7 mode selection 00B: HB7 is in high impedance (default). 01B: LS7 is ON. 10B: HS7 is ON. 11B: Reserved - HB7 is in high impedance.
11:10	HB6MODE	R/W	Half-bridge output 6 mode selection 00B: HB6 is in high impedance (default). 01B: LS6 is ON. 10B: HS6 is ON. 11B: Reserved - HB6 is in high impedance.
9:8	HB5MODE	R/W	Half-bridge output 5 mode selection 00B: HB5 is in high impedance (default). 01B: LS5 is ON. 10B: HS5 is ON. 11B: Reserved - HB5 is in high impedance.
7:6	HB4MODE	R/W	Half-bridge output 4 mode selection 00B: HB4 is in high impedance (default). 01B: LS4 is ON. 10B: HS4 is ON. 11B: Reserved - HB4 is in high impedance.
5:4	HB3MODE	R/W	Half-bridge output 3 mode selection 00B: HB3 is in high impedance (default). 01B: LS3 is ON. 10B: HS3 is ON. 11B: Reserved - HB3 is in high impedance.
3:2	HB2MODE	R/W	Half-bridge output 2 mode selection 00B: HB2 is in high impedance (default). 01B: LS2 is ON. 10B: HS2 is ON. 11B: Reserved - HB2 is in high impedance.
1:0	HB1MODE	R/W	Half-bridge output 1 mode selection 00B: HB1 is in high impedance (default). 01B: LS1 is ON. 10B: HS1 is ON. 11B: Reserved - HB1 is in high impedance.

8.2.9 SETTING OF PWM CHANNELS

PWMSET PWM channel settings (0 0111B:)Reset Value: 0110 1100 0110 0000B:

Table 25. PWM Channel Settings

BIT	FIELD	TYPE	DESCRIPTION
15	Reserved	R	Reserved. Always read as '0'
14	PASS_VDS	R/W	Drain-Source monitoring in bridge passive mode 0B: DS monitoring in bridge passive mode disabled 1B: DS monitoring in bridge passive mode enabled (default)
13:12	PASS_MOD	R/W	Settings for bridge driver passive mode 00B: LS1-4 are always off. Note: Changing PASS_MOD from 00B: to any other value requires to clear DSOV1) first before writing PASS_MOD, 01B: LS1-4 are always on (static brake). 10B: LS1-4 are activated if passive VM OV is detected (overvoltage brake) (default). 11B: LS1-4 are activated if passive VM OV is detected and PWM1 = High (overvoltage brake conditioned by PWM1).
11:9	PWM3_HB	R/W	Allocation of the PWM channel 3 000B: HB1 001B: HB2 010B: HB3 011B: HB4 100B: HB5 101B: HB6 110B: HB7 (default) 111B: HB8
8	PWM3_EN	R/W	PWM channel 3 enable 0B: PWM3 is disabled (default). 1B: PWM3 is enabled.
7:5	PWM2_HB	R/W	Allocation of the PWM channel 2 000B: HB1 001B: HB2 010B: HB3 011B: HB4 (default) 100B: HB5 101B: HB6 110B: HB7 111B: HB8
4	PWM2_EN	R/W	PWM channel 2 enable 0B: PWM2 is disabled (default). 1B: PWM2 is enabled.
3:1	PWM1_HB	R/W	Allocation of the PWM channel 1 000B: HB1 (default) 001B: HB2 010B: HB3 011B: HB4 100B: HB5 101B: HB6 110B: HB7 111B: HB8
0	PWM1_EN	R/W	PWM channel 1 enable 0B: PWM1 is disabled (default). 1B: PWM1 is enabled.

Note: If DSOV is not cleared first, the value of PASS_MOD stays at 00B.

8.2.10 PWM PRE-CHARGE AND PREDISCHARGE TIME

TPRECHG Charge and pre-charge time (0 1000B:) Reset Value: 0B:

Table 26. Charge and Pre-Charge Time

BIT	FIELD	TYPE	DESCRIPTION
15	Reserved	R/W	Reserved. To be programmed as '0'.
14	EN_DEEP_A D	R/W	Reserved
13	Reserved	R/W	Reserved. This bit must be set to '0'.
12	EN_GEN_CH ECK	R/W	Enable generator check 0B: Detection of generator mode disabled (default) 1B: Detection of generator mode enabled
11:10	TPDCHG3	R/W	Pre-discharge time of PWM channel 3 00B: 125ns (default) 01B: 250ns 10B: 500ns 11B: 1000ns
9:8	TPCHG3	R/W	Pre-charge time of PWM channel 3 00B: 125ns (default) 01B: 250ns 10B: 500ns 11B: 1000ns
7:6	TPDCHG2	R/W	Pre-discharge time of PWM channel 2 00B: 125ns (default) 01B: 250ns 10B: 500ns 11B: 1000ns
5:4	TPCHG2	R/W	Pre-charge time of PWM channel 2 00B: 125ns (default) 01B: 250ns 10B: 500ns 11B: 1000ns
3:2	TPDCHG1	R/W	Pre-discharge time of PWM channel 1 00B: 125ns (default) 01B: 250ns 10B: 500ns 11B: 1000ns
1:0	TPCHG1	R/W	Pre-charge time of PWM channel 1 00B: 125ns (default) 01B: 250ns 10B: 500ns 11B: 1000ns

8.2.11 HALF-BRIDGE DIAGNOSTIC CURRENT CONTROL

HBIDIAG Half-bridge diagnostic current control (0 1001B:)Reset Value: 1100 0000 0000 0000B:

Table 27. Half-Bridge Diagnostic Current Control

BIT	FIELD	TYPE	DESCRIPTION
15	CSA2L	R/W	Level of current sense amplifier 2 0B: Current sense amplifier 2 is configured as low-side. 1B: Current sense amplifier 2 is configured as high-side (default).
14	CSA1L	R/W	Level of current sense amplifier 1 0B: Current sense amplifier 1 is configured as low-side. 1B: Current sense amplifier 1 is configured as high-side (default).
13:12	OC2FILT	R/W	Overcurrent filter time for SO2 00B: 6μs (default) 01B: 10μs 10B: 50μs 11B: 100μs
11:10	OC1FILT	R/W	Overcurrent filter time for SO1 00B: 6μs (default) 01B: 10μs 10B: 50μs 11B: 100μs
9	CSA2_OFF	R/W	Disable of current sense amplifier 2 0B: Current sense amplifier 2 enabled (default) 1B: Current sense amplifier 2 disabled
8	CSA1_OFF	R/W	Disable of current sense amplifier 1 0B: Current sense amplifier 1 enabled (default) 1B: Current sense amplifier 1 disabled
7	HB8IDIAG	R/W	Control of HB8 off-state current source and current sink 0B: Pull-down deactivated (default) 1B: Pull-down activated
6	HB7IDIAG	R/W	Control of HB7 off-state current source and current sink 0B: Pull-down deactivated (default) 1B: Pull-down activated
5	HB6IDIAG	R/W	Control of HB6 off-state current source and current sink 0B: Pull-down deactivated (default) 1B: Pull-down activated
4	HB5IDIAG	R/W	Control of HB5 off-state current source and current sink 0B: Pull-down deactivated (default) 1B: Pull-down activated
3	HB4IDIAG	R/W	Control of HB4 off-state current source and current sink 0B: Pull-down deactivated (default) 1B: Pull-down activated
2	HB3IDIAG	R/W	Control of HB3 off-state current source and current sink 0B: Pull-down deactivated (default) 1B: Pull-down activated
1	HB2IDIAG	R/W	Control of HB2 off-state current source and current sink 0B: Pull-down deactivated (default) 1B: Pull-down activated
0	HB1IDIAG	R/W	Control of HB1 pull-down for off-state diagnostic 0B: Pull-down deactivated (default) 1B: Pull-down activated

8.2.12 CHARGE CURRENT FOR STATIC HALFBRIDGES

ST_ICHG Static charge and discharge current selection (0 1010B:)Reset Value: 0000 0000 0100 0100B:

Table 28. Static Charge and Discharge Current Selection

BIT	FIELD	TYPE	DESCRIPTION
14	HB7ICHGST	R/W	HB7 selection of charge and discharge currents 0B: The static charge/discharge current 1 is applied to the half-bridge 7 (default). 1B: The static charge/discharge current 2 is applied to the half-bridge 7.
13	HB6ICHGST	R/W	HB6 selection of charge and discharge currents 0B: The static charge/discharge current 1 is applied to the half-bridge 6 (default). 1B: The static charge/discharge current 2 is applied to the half-bridge 6.
12	HB5ICHGST	R/W	HB5 selection of charge and discharge currents 0B: The static charge/discharge current 1 is applied to the half-bridge 5 (default). 1B: The static charge/discharge current 2 is applied to the half-bridge 5.
11	HB4ICHGST	R/W	HB4 selection of charge and discharge currents 0B: The static charge/discharge current 1 is applied to the half-bridge 4 (default). 1B: The static charge/discharge current 2 is applied to the half-bridge 4.
10	HB3ICHGST	R/W	HB3 selection of charge and discharge currents 0B: The static charge/discharge current 1 is applied to the half-bridge 3 (default). 1B: The static charge/discharge current 2 is applied to the half-bridge 3.
9	HB2ICHGST	R/W	HB2 selection of charge and discharge currents 0B: The static charge/discharge current 1 is applied to the half-bridge 2 (default). 1B: The static charge/discharge current 2 is applied to the half-bridge 2.
8	HB1ICHGST	R/W	HB1 selection of charge and discharge currents 0B: The static charge/discharge current 1 is applied to the half-bridge 1 (default). 1B: The static charge/discharge current 2 is applied to the half-bridge 1.
7:4	ICHGST2	R/W	Static gate driver charge and discharge currents 2 Refer to Table 10 0100B (default): Charge 12.5mA typ., discharge 14.2mA typ.
3:0	ICHGST1	R/W	Static gate driver charge and discharge currents 1 Refer to Table 10 0100B (default): Charge 12.5mA typ., discharge 14.2mA typ.

8.2.13 PRECHARGE CURRENT INITIALIZATION

PWM_PCHG_INIT Initial PWM precharge current selection (0 1010B:)Reset Value: 0001 1000 1100 0110B:

Table 29. Initial PWM Precharge Current Selection

BIT	FIELD	TYPE	DESCRIPTION
15	Reserved	R	Reserved. Always read as '0'.
14:10	PCHGINIT3	R/W	Initial precharge current of PWM channel 3 Refer to Table 13 00110B (default): 8.0mA typ.
9:5	PCHGINIT2	R/W	Initial precharge current of PWM channel 2 Refer to Table 13 00110B (default): 8.0mA typ.
4:0	PCHGINIT1	R/W	Initial precharge current of PWM channel 1 Refer to Table 13 00110B (default): 8.0mA typ.

8.2.14 CHARGE CURRENT FOR HALF-BRIDGES IN PWM (ACTIVE MOSFETS1)

PWM_ICHG_ACT Active PWM charge current (0 1011B:)Reset Value:0001 1000 1100 0110B:

Table 30. Active PWM Charge Current

BIT	FIELD	TYPE	DESCRIPTION
15	Reserved	R	Reserved. Always read as '0'
14:10	ICHG3	R/W	Gate driver charge current of PWM channel 3 (active MOSFET) Refer to Table 13 00110B (default): 8.0mA typ.
9:5	ICHG2	R/W	Gate driver charge current of PWM channel 2 (active MOSFET) Refer to Table 13 00110B (default): 8.0mA typ.
4:0	ICHG1	R/W	Gate driver charge current of PWM channel 1 (active MOSFET) Refer to Table 13 00110B (default): 8.0mA typ.

8.2.15 CHARGE CURRENT FOR HALF-BRIDGES IN PWM (FW MOSFETS1)

PWM_ICHG_FW FW PWM charge/discharge currents (0 1011B:) Reset Value:0001 1000 1100 0110B:

Table 31. PWM Charge/Discharge Currents

BIT	FIELD	TYPE	DESCRIPTION
15	Reserved	R	Reserved. Always read as '0'.
14:10	ICHG3_FW	R/W	Gate driver charge and discharge currents of PWM channel 3 (FW MOSFET) Refer to Table 13, Table 14 00110B (default): Charge 8.0mA typ., discharge 9.4mA typ.
9:5	ICHG2_FW	R/W	Gate driver charge and discharge currents of PWM channel 2 (FW MOSFET) Refer to Table 13, Table 14 00110B (default): Charge 8.0mA typ., discharge 9.4mA typ.
4:0	ICHG1_FW	R/W	Gate driver charge and discharge currents of PWM channel 1 (FW MOSFET) Refer to Table 13, Table 14 00110B (default): Charge 8.0mA typ., discharge 9.4mA typ.

8.2.16 DISCHARGE CURRENT OF ACTIVE MOSFETS1) IN PWM OPERATION

PWM_IDCHG_ACT PWM discharge current (0 1100B:)Reset Value: 0001 1100 1110 0111B:

Table 32. PWM Discharge Current

BIT	FIELD	TYPE	DESCRIPTION
15	CCSO	R/W	Reserved.
14:10	IDCHG3	R/W	Discharge current for PWM channel 3 (active MOSFET) Refer to Table 14 00111B (default): 11.8mA typ.
9:5	IDCHG2	R/W	Discharge current for PWM channel 2 (active MOSFET) Refer to Table 14 00111B (default): 11.8mA typ.
4:0	IDCHG1	R/W	Discharge current of PWM channel 1 (active MOSFET) Refer to Table 14 00111B (default): 11.8mA typ.

8.2.17 PREDISCHARGE CURRENT INITIALIZATION

PWM_PDCHG_INIT Initial PWM predischarge current selection (0 1100B:)Reset Value: 0011 0001 1000 1100B:

Table 33. ???

BIT	FIELD	TYPE	DESCRIPTION
15	CCSO	R/W	Reserved
14:10	PDCHGINIT 3	R/W	Initial predischarge current of PWM channel 3 Refer to Table 14 01100B (default): 26.0mA typ.
9:5	PDCHGINIT 2	R/W	Initial predischarge current of PWM channel 2 Refer to Table 14 01100B (default): 26.0mA typ.
4:0	PDCHGINIT 1	R/W	Initial predischarge current of PWM channel 1 Refer to Table 14 01100B (default): 26.0mA typ.

8.2.18 MAX. PRE-CHARGE / PRE-DISCHARGE CURRENTS FOR HALF-BRIDGES IN PWM2), TCCP AND TBLANK SETTING FOR ACTIVE MOSFETS1)

PWM_ICHGMAX_CCP_BLK3_ACT PWM max. drive current (0 1101B:)Reset Value: 0100 1001 0000 0000B:

Table 34. ???

BIT	FIELD	TYPE	DESCRIPTION
15	Reserved	R	Reserved. Always read as '0'.
14:12	TBLANK4_ACT	R/W	Blank time 1 - tBLANK4 active Refer to Table 30
11:9	TCCP4_ACT	R/W	Cross-current protection 1 - tCCP4 active Refer to Table 29 100B (default): 2000ns typ.
8:6	TBLANK3_ACT	R/W	Blank time 1 - tBLANK3 active Refer to Table 30 100B (default): 2000ns typ.
5:4	ICHGMAX3	R/W	Maximum drive current of half-bridge mapped to PWM channel 3 during the pre-charge phase and pre-discharge phases 2 00B (default): Charge 18.8mA typ., discharge 19.7mA typ. 01B: Charge 41mA typ., discharge 43mA typ. 10B: Charge 77mA typ., discharge 79mA typ. 11B: Charge 100mA typ., discharge 100mA typ.
3:2	ICHGMAX2	R/W	Maximum drive current of half-bridge mapped to PWM channel 2 during the pre-charge phase and pre-discharge phases 2) 00B (default): Charge 18.8mA typ., discharge 19.7mA typ. 01B: Charge 41mA typ., discharge 43mA typ. 10B: Charge 77mA typ., discharge 79mA typ. 11B: Charge 100mA typ., discharge 100mA typ.
1:0	ICHGMAX1	R/W	Maximum drive current of half-bridge mapped to PWM channel 1 during the pre-charge and pre-discharge phases 2) 00B (default): Charge 18.8mA typ., discharge 19.7mA typ. 01B: Charge 41mA typ., discharge 43mA typ. 10B: Charge 77mA typ., discharge 79mA typ. 11B: Charge 100mA typ., discharge 100mA typ.

8.2.19 MAX. PRE-CHARGE / PRE-DISCHARGE CURRENTS FOR HALF-BRIDGES IN PWM2), TCCP AND TBLANK SETTING FOR FW MOSFETS1)

PWM_ICHGMAX_CCP_BLK3_FW PWM max. drive current (0 1101B:)Reset Value: 0100 1001 0000 0000B:

Table 35. ???

BIT	FIELD	TYPE	DESCRIPTION
15	Reserved	R	Reserved. Always read as '0'.
14:12	TBLANK4_F W	R/W	Blank time 1 - tBLANK4 freewheeling Refer to Table 32 100B (default): 2000ns typ.
11:9	TCCP4_FW	R/W	Cross-current protection 1 - tCCP4 freewheeling Refer to Table 31 100B (default): 2000ns typ.
8:6	TBLANK3_F W	R/W	Blank time 1 - tBLANK3 Freewheeling Refer to Table 32 100B (default): 2000ns typ.
5:4	ICHGMAX3	R/W	Maximum drive current of half-bridge mapped to PWM channel 3 during the pre-charge phase and pre-discharge phases 2 00B (default): Charge 19mA typ., discharge 19mA typ. 01B: Charge 41mA typ., discharge 43mA typ. 10B: Charge 77mA typ., discharge 79mA typ. 11B: Charge 100mA typ., discharge 100mA typ.
3:2	ICHGMAX2	R/W	Maximum drive current of half-bridge mapped to PWM channel 2 during the pre-charge phase and pre-discharge phases 2 00B (default): Charge 19mA typ., discharge 19mA typ. 01B: Charge 41mA typ., discharge 43mA typ. 10B: Charge 77mA typ., discharge 79mA typ. 11B: Charge 100mA typ., discharge 100mA typ.
1:0	ICHGMAX1	R/W	Maximum drive current of half-bridge mapped to PWM channel 1 during the pre-charge and pre-discharge phases 2 00B (default): Charge 19mA typ., discharge 19mA typ. 01B: Charge 41mA typ., discharge 43mA typ. 10B: Charge 77mA typ., discharge 79mA typ. 11B: Charge 100mA typ., discharge 100mA typ.

8.2.20 TURN-ON AND TURN-OFF DELAYS FOR PWM CHANNEL1

TDON_OFF1 MOSFET turn-on/off delay of PWM channel 1 (0 1110B:)Reset Value:0000 1010 0000 1010B:

Table 36. Turn-On/Off Delay of PWM Channel 1

BIT	FIELD	TYPE	DESCRIPTION
15:8	TDOFF1	R/W	Turn-off delay time of PWM channel 1 Typical TDOFF1 = 62.5 × TDOFF1(7:0)Dns 0000 1010B (default): 625ns typ.
7:0	TDON1	R/W	Turn-on delay time of PWM channel 1 Typical TDON1 = 62.5 × TDON1(7:0)Dns 0000 1010B (default): 625ns typ.

8.2.21 TURN-ON AND TURN-OFF DELAYS FOR PWM CHANNEL2

TDON_OFF2 MOSFET turn-on/off delay of PWM channel2 (0 1111B:)Reset Value: 0000 1010 0000 1010B:

Table 37.

BIT	FIELD	TYPE	DESCRIPTION
15:8	TDOFF2	R/W	Turn-off delay time of PWM channel 2 Typical TDOFF2 = 62.5 × TDOFF2(7:0)Dns 0000 1010B (default): 625ns typ.
7:0	TDON2	R/W	Turn-on delay time of PWM channel 2 Typical TDON2 = 62.5 x TDON2(7:0)Dns 0000 1010B (default): 625ns typ.

8.2.22 TURN-ON AND TURN-OFF DELAYS FOR PWM CHANNEL3

TDON_OFF3 MOSFET turn-on/off delay of PWM channel3 (1 0000B:)Reset Value: 0000 1010 0000 1010B:

Table 38.

BIT	FIELD	TYPE	DESCRIPTION
15:8	TDOFF3	R/W	Turn-off delay time of PWM channel 3 Typical TDOFF3 = 62.5 × TDOFF3(7:0)Dns Default: 0000 1010B: 625ns typ.
7:0	TDON3	R/W	Turn-on delay time of PWM channel 3 Typical TDON3 = 62.5 × TDON3(7:0)Dns 0000 1010B (default): 625ns typ.

8.2.23 HALF BRIDGES DRV LOW POWER MODE ENABLE AND HIGH HARDOFF CURRENT ENABLE

Half bridges drv low power mode enable and high hardoff current enable (1_1100B:)Reset Value: 0000 0010 0000 0000B:

Table 39.

BIT	FIELD	TYPE	DESCRIPTION
15	GDF_EN	R/W	Note：this bit must be always 0 if the SPI is used as daisy chain 1: enable to report a gate driver fault for each HS and LS mosfet to the status register GDF(0x1A) and the SPI global status byte bit7. 0: status register GDF(0x1A) and the SPI global status byte bit7 are always zero. (default)
14	OSC_SSC_DIS	R/W	1: disable the internal OSC spectrum spread 0: enable the internal OSC spectrum spread.(default)
13	PDR_DIS	R/W	1: disable the IPRECHARGE and IPREDISCHARGE current adaptive control when AGC= 2'b10 or 2'b11 0: enable the IPRECHARGE and IPREDISCHARGE current adaptive control when AGC= 2'b10 or 2'b11(default)
12	STC_EN	R/W	1: enable the slew time adaptive control, adjust the trise and tafll time to the target set in TRISE_FALL bits, the charge and discharge current adaptation step could by configured by IPCHGADT, and the slew time adaptive control filter could be enabled or disabled by AGCFLT. 0: disable the slew time adaptive control(default)
11:8	TRISE_FALL	R/W	4'h0: trise_fall_exp = 6 * 62.5ns; 4'h1: trise_fall_exp = 9* 62.5; 4'h2: trise_fall_exp = 12* 62.5;(default) 4'h3: trise_fall_exp = 16;* 62.5 4'h4: trise_fall_exp = 21* 62.5; 4'h5: trise_fall_exp = 26* 62.5; 4'h6: trise_fall_exp = 32* 62.5;

			4'h7: trise_fall_exp = 39* 62.5; 4'h8: trise_fall_exp = 47* 62.5; 4'h9: trise_fall_exp = 64* 62.5; 4'ha: trise_fall_exp = 80* 62.5; 4'hb: trise_fall_exp = 95* 62.5; 4'hc: trise_fall_exp = 128* 62.5; 4'hd: trise_fall_exp = 159* 62.5; 4'he: trise_fall_exp = 191;* 62.5 4'hf: trise_fall_exp = 255* 62.5;
7:2	Reserved	R	Reserved
1	DRV_HARDOFF_EN	R/W	1: enable the larger hardoff current for each half bridge 0: disable the larger hardoff current for each half bridge(default)
0	DRV_LPWR_EN	R/W	1: enable the low power mode for the half bridge, the driver and OCP of the half bridge is disable if the HBxMODE =2'00/2'b11. 0: disable the low power mode for the half bridge, the driver and OCP of the half bridge will be still enabled even the HBxMODE = 2'00/2'b11.(default)

8.2.24 HALF BRIDGES OC AND SH CONFIGURATION FOR CSA1 AND CSA2

Half bridges OC and SH configuration for CSA1 and CSA2 (1_1101B:)Reset Value: 0000 0000 0000 0000B:

Table 40.

BIT	FIELD	TYPE	DESCRIPTION
15:11	Reserved	R	Reserved
10	HB6_PWM4	R/W	1: enable EN pin as PWM4 function 0: disable EN pin as PWM4 function(default)
9	CSA_BLK_SEL	R/W	1: CSA1 and CSA2 hold blank time is tccp + tblank/2 0: CSA1 and CSA2 hold blank time is tccp + tblank(default)
8	CSA2_SH_EN	R/W	1: CSA2 sample and hold function is enable, CSA2 output hold between the cross-current protection time and the the hold blank time configured by CSA_BLK_SEL. 0: CSA2 is always sampled.(default)
7	CSA1_SH_EN	R/W	1: CSA1 sample and hold function is enable, CSA2 output holds between the cross-current protection time and the hold blank time configured by CSA_BLK_SEL. 0: CSA1 is always sampled.(default)
6	OC_SEP_EN	R/W	1: only the connected half bridge is turn off by CSA1 and CSA2 OC even when OCEN =1. 0: All half bridges are turn off by CSA1 and CSA2 OC even when OCEN =1.
5:3	CSA2_SEL	R/W	3'h0: CSA2 is connected to HB1 3'h1: CSA2 is connected to HB2 3'h2: CSA2 is connected to HB3 3'h3: CSA2 is connected to HB4 3'h4: CSA2 is connected to HB5 3'h5: CSA2 is connected to HB6 3'h6: CSA2 is connected to HB7 3'h7: CSA2 is connected to HB8
2:0	CSA1_SEL	R/W	3'h0: CSA1 is connected to HB1 3'h1: CSA1 is connected to HB2 3'h2: CSA1 is connected to HB3 3'h3: CSA1 is connected to HB4 3'h4: CSA1 is connected to HB5 3'h5: CSA1 is connected to HB6 3'h6: CSA1 is connected to HB7 3'h7: CSA1 is connected to HB8

8.2.25 MISC FUNCTIONS CONFIGURATION

MISC functions configuration (1_1110B:) Reset Value: 0000 0000 0000 0000B:

Table 41.

BIT	FIELD	TYPE	DESCRIPTION
15:14	Reserved	R	Reserved
13	VCP_SHORT_DIS	R/W	1: disable the vcp short protection(default) 0: enable the vcp short protection
12	HAND_SHAKE_DIS	R/W	1: disable the internal handshake dead-time 0: enable the internal handshake dead-time(default)
11	VCP_FORCE_ONE_STAGE	R/W	1: force the vcp work in single mode 0: back to (CFG_VCP_STGA、VM_OV16V) control mode
10	VCP_SYNC_MODE	R/W	0: disable the stop switch sync with clk 1: enable the stop switch sync with the clk（default）
9	VCP_NOHYST	R/W	1: disable VCP hysteresis 0: enable VCP hysteresis(default)
8	VDS_SETL	R/W	1: All HB drain-source monitoring threshold is half of the value configured by VDS1 and VDS2 0: All HB drain-source monitoring threshold is the value configured by VDS1 and VDS2
7	DIS_HB8_FW	R/W	1: the HB8 freewheeling mosfet will be always turned off 0: the HB8 freewheeling mosfet could be turned on by pwm(default)
6	DIS_HB7_FW	R/W	1: the HB7 freewheeling mosfet will be always turned off 0: the HB7 freewheeling mosfet could be turned on by pwm(default)
5	DIS_HB6_FW	R/W	1: the H6 freewheeling mosfet will be always turned off 0: the HB6 freewheeling mosfet could be turned on by pwm(default)
4	DIS_HB5_FW	R/W	1: the HB5 freewheeling mosfet will be always turned off 0: the HB5 freewheeling mosfet could be turned on by pwm(default)
3	DIS_HB4_FW	R/W	1: the HB4 freewheeling mosfet will be always turned off 0: the HB4 freewheeling mosfet could be turned on by pwm(default)
2	DIS_HB3_FW	R/W	1: the HB3 freewheeling mosfet will be always turned off 0: the HB3 freewheeling mosfet could be turned on by pwm(default)
1	DIS_HB2_FW	R/W	1: the HB2 freewheeling mosfet will be always turned off 0: the HB2 freewheeling mosfet could be turned on by pwm(default)
0	DIS_HB1_FW	R/W	1: the HB1 freewheeling mosfet will be always turned off 0: the HB1 freewheeling mosfet could be turned on by pwm(default)

8.3 STATUS REGISTER

Table 42. Overview

REGISTER LONG NAME	REGISTER SHORT NAME	OFFSET ADDRESS	RESET VALUE
General Status Register	GENSTAT	11H	0H
Drain-Source Overvoltage	DSOV	12H	0H
Half-Bridge Output Voltage	HBVOUT_PWMERR	13H	0H
Effective MOSFET Turn-On and Turn-Off Delays for PWM Channel 1	EFF_TDON_OFF1	14H	0H
Effective MOSFET Turn-On and Turn-Off Delays for PWM Channel 2	EFF_TDON_OFF2	15H	0H
Effective MOSFET turn-On and Turn-Off Delays for PWM Channel 3	EFF_TDON_OFF3	16H	0H
Effective MOSFET Rise and Fall Times for PWM Channel 1	TRISE_FALL1	17H	0H
Effective MOSFET Rise and Fall Times for PWM Channel 2	TRISE_FALL2	18H	0H
Effective MOSFET Rise and Fall Times for PWM Channel 3	TRISE_FALL3	19H	0H
Gate Driver Fault	GDF	1AH	0H
Device Identifier	DEVID	1FH	01H

8.3.1 GENERAL STATUS REGISTER

GENSTAT General Status Register (1 0001B:)Reset Value: 0B:

Table 43. General Status Register

BIT	FIELD	TYPE	DESCRIPTION
15	PASS_VDSOV	R	DS overvoltage while the bridge driver is in passive mode. 0B: No overvoltage on drain-source of any low side (default) 1B: Overvoltage on drain-source of one of the low-side is detected.
14:13	WDMON	R	Watchdog monitoring 00B: WD Timer is between 0% and 25% of the WD period (default). 01B: WD Timer is between 25% and 50% of the WD period. 10B: WD Timer is between 50% and 75% of the WD period. 11B: WD Timer is between 75% and 100% of the WD period.
12	PWM3STAT	R	Status of PWM3 input 0B: PWM3 is low (default). 1B: PWM3 is high.
11	PWM2STAT	R	Status of PWM2 input 0B: PWM2 is low (default). 1B: PWM2 is high.
10	PWM1STAT	R	Status of PWM1 input 0B: PWM1 is low (default). 1B: PWM1 is high.
9	TDREG3	rc	PWM channel 3 - Regulation of turn-on and turn-off delays 0B: The turn-on delay or the turn-off delay are not in regulation (default). 1B: The turn-on and turn-off delays are in regulation.
8	TDREG2	rc	PWM channel 2 - Regulation of turn-on and turn-off delays 0B: The turn-on delay or the turn-off delay are not in regulation (default). 1B: The turn-on and turn-off delays are in regulation.
7	TDREG1	rc	PWM channel 1 - Regulation of turn-on and turn-off delays 0B: The turn-on delay or the turn-off delay are not in regulation (default). 1B: The turn-on and turn-off delays are in regulation.
6	TSD	rc	Thermal shutdown 0B: No thermal shutdown is detected (default). 1B: A thermal shutdown is detected.

BIT	FIELD	TYPE	DESCRIPTION
5	TW	rc	Thermal warning 0B: No thermal warning is detected (default). 1B: A thermal warning is detected.
4	OC2	rc	Overcurrent detection of SO2 0B: No overcurrent detection on SO2 (default) 1B: Overcurrent detected on SO21
3	OC1	rc	Overcurrent detection of SO1 0B: No overcurrent detection on SO1 (default) 1B: Overcurrent detected on SO1
2	VSOV	rc	VM overvoltage 0B: No overvoltage on VM detected (default) 1B: Overvoltage on VM detected
1	VSUV	rc	VM undervoltage 0B: No undervoltage on VM detected (default) 1B: Undervoltage on VM detected
0	CPUV	rc	Charge pump undervoltage 0B: No charge pump undervoltage (default) 1B: A charge pump undervoltage is detected

8.3.2 DRAIN-SOURCE OVERVOLTAGE

DSOV

Drain-Source Overvoltage (1 0010B:)Reset Value: 0B:

Table 44.

BIT	FIELD	TYPE	DESCRIPTION
15	LS8DSOV	rc	Drain-source overvoltage on low-side 8 0B: No overvoltage on drain-source of low-side 8 (default) 1B: Overvoltage on drain-source of low-side 8 detected
14	HS8DSOV	rc	Drain-source overvoltage on high-side 8 0B: No overvoltage on drain-source of high-side 8 (default) 1B: Overvoltage on drain-source of high-side 8 detected.
13	LS7DSOV	rc	Drain-source overvoltage on low-side 7 0B: No overvoltage on drain-source of low-side 7 (default) 1B: Overvoltage on drain-source of low-side 7 detected.
12	HS7DSOV	rc	Drain-source overvoltage on high-side 7 0B: No overvoltage on drain-source of high-side 7 (default) 1B: Overvoltage on drain-source of high-side 7 detected.
11	LS6DSOV	rc	Drain-source overvoltage on low-side 6 0B: No overvoltage on drain-source of low-side 6 (default) 1B: Overvoltage on drain-source of low-side 6 detected.
10	HS6DSOV	rc	Drain-source overvoltage on high-side 6 0B: No overvoltage on drain-source of high-side 6 (default) 1B: Overvoltage on drain-source of high-side 6 detected.
9	LS5DSOV	rc	Drain-source overvoltage on low-side 5 0B: No overvoltage on drain-source of low-side 5 (default) 1B: Overvoltage on drain-source of low-side 5 detected.
8	HS5DSOV	rc	Drain-source overvoltage on high-side 5 0B: No overvoltage on drain-source of high-side 5 (default) 1B: Overvoltage on drain-source of high-side 5 detected.
7	LS4DSOV	rc	Drain-source overvoltage on low-side 4 0B: No overvoltage on drain-source of low-side 4 (default) 1B: Overvoltage on drain-source of low-side 4 detected.
6	HS4DSOV	rc	Drain-source overvoltage on high-side 4 0B: No overvoltage on drain-source of high-side 4 (default) 1B: Overvoltage on drain-source of high-side 4 detected.

BIT	FIELD	TYPE	DESCRIPTION
5	LS3DSOV	rc	Drain-source overvoltage on low-side 3 0B: No overvoltage on drain-source of low-side 3 (default) 1B: Overvoltage on drain-source of low-side 3 detected.
4	HS3DSOV	rc	Drain-source overvoltage on high-side 3 0B: No overvoltage on drain-source of high-side 3 (default) 1B: Overvoltage on drain-source of high-side 3 detected.
3	LS2DSOV	rc	
2	HS2DSOV	rc	Drain-source overvoltage on high-side 2 0B: No overvoltage on drain-source of high-side 2 (default) 1B: Overvoltage on drain-source of high-side 2 detected.
1	LS1DSOV	rc	Drain-source overvoltage on low-side 1 0B: No overvoltage on drain-source of low-side 1 (default) 1B: Overvoltage on drain-source of low-side 1 detected.
0	HS1DSOV	rc	Drain-source overvoltage on high-side 1 0B: No overvoltage on drain-source of high-side 1 (default) 1B: Overvoltage on drain-source of high-side 1 detected.

8.3.3 HALF-BRIDGE OUTPUT VOLTAGE

HBVOUT_PWMERR

Half-bridge output voltage and PWM error (1 0011B:)Reset Value: 0B:

Table 45.

BIT	FIELD	TYPE	DESCRIPTION
15	HB8PWME	R	PWM error on HB8 0B: No PWM error (default) 1B: More than one activated PWM channels is mapped to HB81.
14	HB7PWME	R	PWM error on HB7 0B: No PWM error (default) 1B: More than one activated PWM channels is mapped to HB71.
13	HB6PWME	R	PWM error on HB6 0B: No PWM error (default) 1B: More than one activated PWM channels is mapped to HB61.
12	HB5PWME	R	PWM error on HB5 0B: No PWM error (default) 1B: More than one activated PWM channels is mapped to HB51.
11	HB4PWME	R	PWM error on HB4 0B: No PWM error (default) 1B: More than one activated PWM channels is mapped to HB41.
10	HB3PWME	R	PWM error on HB3 0B: No PWM error (default) 1B: More than one activated PWM channels is mapped to HB31.
9	HB2PWME	R	PWM error on HB2 0B: No PWM error (default) 1B: More than one activated PWM channels is mapped to HB21.
8	HB1PWME	R	PWM error on HB1 0B: No PWM error (default) 1B: More than one activated PWM channels is mapped to HB11.
7	HB8VOUT	R	Voltage level at SH8 when HB8MODE(1:0) = (0, 0) or (1, 1) 0B: Low: |VDH – VSH8| > VVDSMONTHx if HB8D = 0 |VCSIN1 – VSH8| > VVDSMONTHx if HB8D = 1 1B: High: |VDH – VSH8| < VVDSMONTHx if HB8D = 0; |VCSIN1 – VSH8| < VVDSMONTHx if HB8D = 1 Note: HB8VOUT = 0 if HB8MODE(1:0)= (0, 1) or (1, 0)
6	HB7VOUT	R	Voltage level at SH7 when HB7MODE(1:0) = (0, 0) or (1, 1) 0B: Low: |VDH – VSH7| > VVDSMONTHx if HB7D = 0

			|VCSIN1 – VSH7| > VVDSMONTHx if HB7D = 1 1B: High: |VDH – VSH7| < VVDSMONTHx if HB7D = 0; |VCSIN1 – VSH7| < VVDSMONTHx if HB7D = 1 Note: HB7VOUT = 0 if HB7MODE(1:0)= (0, 1) or (1, 0)
5	HB6VOUT	R	Voltage level at SH6 when HB6MODE(1:0) = (0, 0) or (1, 1) 0B: Low: |VDH – VSH6| > VVDSMONTHx if HB6D = 0 |VCSIN1 – VSH6| > VVDSMONTHx if HB6D = 1 1B: High: |VDH – VSH6| < VVDSMONTHx if HB6D = 0; |VCSIN1 – VSH6| < VVDSMONTHx if HB6D = 1 Note: HB6VOUT = 0 if HB6MODE(1:0)= (0, 1) or (1, 0)
4	HB5VOUT	R	Voltage level at SH5 when HB5MODE(1:0) = (0, 0) or (1, 1) 0B: Low: |VDH – VSH5| > VVDSMONTHx if HB5D = 0 |VCSIN1 – VSH5| > VVDSMONTHx if HB5D = 1 1B: High: |VDH – VSH5| < VVDSMONTHx if HB5D = 0; |VCSIN1 – VSH5| < VVDSMONTHx if HB5D = 1 Note: HB5VOUT = 0 if HB5MODE(1:0)= (0, 1) or (1, 0)
3	HB4VOUT	R	Voltage level at SH4 when HB4MODE(1:0) = (0, 0) or (1, 1) 0B: Low: |VDH – VSH4| > VVDSMONTHx if HB4D = 0 |VCSIN1 – VSH4| > VVDSMONTHx if HB4D = 1 1B: High: |VDH – VSH4| < VVDSMONTHx if HB4D = 0; |VCSIN1 – VSH4| < VVDSMONTHx if HB4D = 1 Note: HB4VOUT = 0 if HB4MODE(1:0)= (0, 1) or (1, 0)
2	HB3VOUT	R	Voltage level at SH3 when HB3MODE(1:0) = (0, 0) or (1, 1) 0B: Low: |VDH – VSH3| > VVDSMONTHx if HB3D = 0 |VCSIN1 – VSH3| > VVDSMONTHx if HB3D = 1 1B: High: |VDH – VSH3| < VVDSMONTHx if HB3D = 0; |VCSIN1 – VSH3| < VVDSMONTHx if HB3D = 1 Note: HB3VOUT = 0 if HB3MODE(1:0)= (0, 1) or (1, 0)
1	HB2VOUT	R	Voltage level at SH2 when HB2MODE(1:0) = (0, 0) or (1, 1) 0B: Low: |VDH – VSH2| >VVDSMONTH 2) if HB2D = 0 x |VCSIN1 – VSH2| > VVDSMONTHx if HB2D = 1 1B: High: |VDH – VSH2| < VVDSMONTHx if HB2D = 0; |VCSIN1 – VSH2| < VVDSMONTHx if HB2D = 1 Note: HB2VOUT = 0 if HB2MODE(1:0)= (0, 1) or (1, 0)
0	HB1VOUT	R	Voltage level at SH1 when HB1MODE(1:0) = (0, 0) or (1, 1) 0B: Low: |VDH – VSH1| >VVDSMONTH 2) if HB1D = 0; x |VCSIN1 – VSH1| > VVDSMONTHx if HB1D = 1 1B: High: |VDH – VSH1| < VVDSMONTHx if HB1D = 0; |VCSIN1 – VSH1| < VVDSMONTHx if HB1D = 1 Note: HB1VOUT = 0 if HB1MODE(1:0)= (0, 1) or (1, 0)

8.3.4 EFFECTIVE MOSFET TURN-ON AND TURN-OFF DELAYS FOR PWM CHANNEL 1

EFF_TDON_OFF1

Effective MOSFET turn-on/off delay PWM1 (1 0100B:)Reset Value: 0B:

Table 46.

BIT	FIELD	TYPE	DESCRIPTION
15:8	TDOFF1EFF	R	Effective MOSFET turn-off delay of PWM channel 1 Effective turn-off delay = 62.5 × TDOFF1EFF(7:0)Dns Default: 0B
7:0	TDON1EFF	R	Effective MOSFET turn-on delay of PWM channel 1 Effective turn-on delay = 62.5 × TDON1EFF(7:0)Dns Default: 0B

8.3.5 EFFECTIVE MOSFET TURN-ON AND TURN-OFF DELAYS FOR PWM CHANNEL 2

EFF_TDON_OFF2

Effective MOSFET turn-on/off delay PWM2 (1 0101B:)Reset Value: 0B:

Table 47.

BIT	FIELD	TYPE	DESCRIPTION
15:8	TDOFF2EFF	R	Effective MOSFET turn-off delay of PWM channel 2 Effective turn-off delay = 62.5 × TDOFF2EFF(7:0)Dns Default: 0B
7:0	TDON2EFF	R	Effective MOSFET turn-on delay of PWM channel 2 Effective turn-on delay = 62.5 × TDON2EFF(7:0)Dns Default: 0B

8.3.6 EFFECTIVE MOSFET TURN-ON AND TURN-OFF DELAYS FOR PWM CHANNEL 3

EFF_TDON_OFF3

Effective MOSFET turn-on/off delay PWM3 (1 0110B:)Reset Value: 0B:

Table 48.

BIT	FIELD	TYPE	DESCRIPTION
15:8	TDOFF3EFF	R	Effective MOSFET turn-off delay of PWM channel 3 Effective turn-off delay = 62.5 × TDOFF3EFF(7:0)Dns Default: 0B
7:0	TDON3EFF	R	Effective MOSFET turn-on delay of PWM channel 3 Effective turn-on delay = 62.5 × TDON3EFF(7:0)Dns Default: 0B

8.3.7 EFFECTIVE MOSFET RISE AND FALL TIMES FOR PWM CHANNEL 1

TRISE_FALL1

Effective PWM MOSFET rise and fall times PWM1 (1 0111B:)Reset Value: 0B:

Table 49.

BIT	FIELD	TYPE	DESCRIPTION
15:8	EFF_EFF_TFALL1	R	MOSFET fall time of PWM channel 1 MOSFET fall time = 62.5 × EFF_EFF_TFALL1(7:0)Dns Default: 0B
7:0	EFF_TRISE1	R	MOSFET rise time of PWM channel 1 MOSFET rise time = 62.5 × EFF_TRISE1(7:0)Dns Default: 0B

8.3.8 EFFECTIVE MOSFET RISE AND FALL TIMES FOR PWM CHANNEL 2

TRISE_FALL2

Effective PWM MOSFET rise and fall times PWM2 (1 1000B:)Reset Value: 0B:

Table 50.

BIT	FIELD	TYPE	DESCRIPTION
15:8	EFF_TFALL2	R	MOSFET fall time of PWM channel 2 MOSFET fall time = 62.5 × EFF_TFALL2(7:0)Dns Default: 0B
7:0	EFF_TRISE2	R	MOSFET rise time of PWM channel 2 MOSFET rise time = 62.5 × EFF_TRISE2(7:0)Dns Default: 0B

8.3.9 EFFECTIVE MOSFET RISE AND FALL TIMES FOR PWM CHANNEL 3

TRISE_FALL3

Effective PWM MOSFET rise and fall times PWM3 (1 1001_B:)Reset Value: 0_B:

Table 51. ???

BIT	FIELD	TYPE	DESCRIPTION
15:8	TFALL3	R	MOSFET fall time of PWM channel 3 MOSFET fall time = 62.5 x TFALL3(7:0)Dns Default: 0B
7:0	EFF_TRISE3	R	MOSFET rise time of PWM channel 3 MOSFET rise time = 62.5 x EFF_TRISE3(7:0)Dns Default: 0B

8.3.10 DEVICE IDENTIFIER

DEVID

Device Identifier (1 1111_B:)Reset Value: $0000\,0001_B$:

Table 52.

BIT	FIELD	TYPE	DESCRIPTION
15	Reserved	R	Reserved. Always read as '0'
14:8	Reserved	R	Reserved. Always read as '0'
7	Reserved	R	Reserved. Always read as '0'.
6:5	Reserved	R	Reserved
4:3	Reserved	R	Reserved
2:0	DEV_ID	R	Device derivative identifier 000B: Reserved 001B: DR7808Q 010B: Reserved 011B: Reserved 100B: Reserved 101B: Reserved 110B: Reserved 111B: Reserved

9. 典型应用

请联系类比技术支持获取参考设计，包括评估板设计文件和应用指导。

10. PACKAGE INFORMATION

The DR7808Q is available in the QFN-48 package. Figure 4 shows the package view.

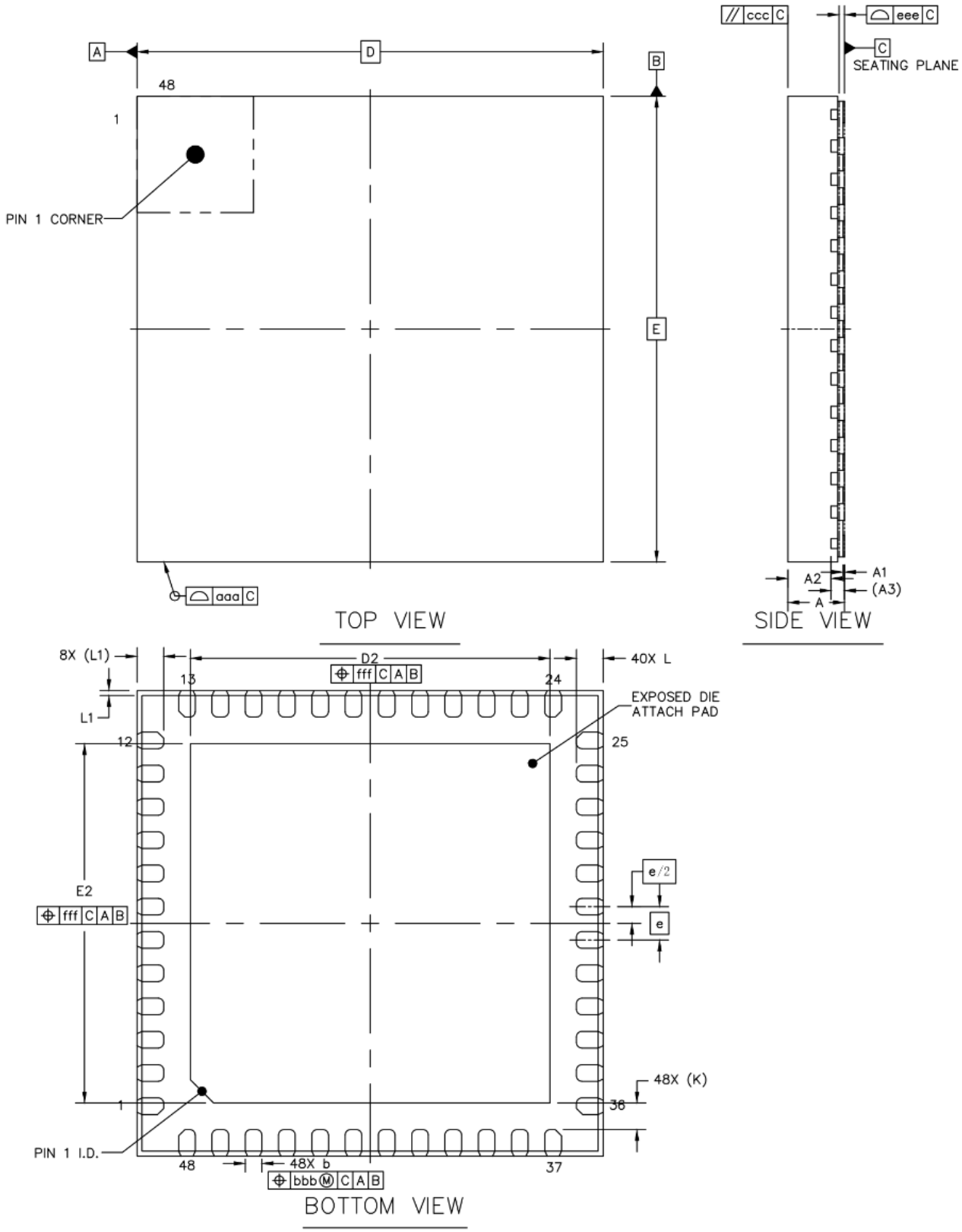


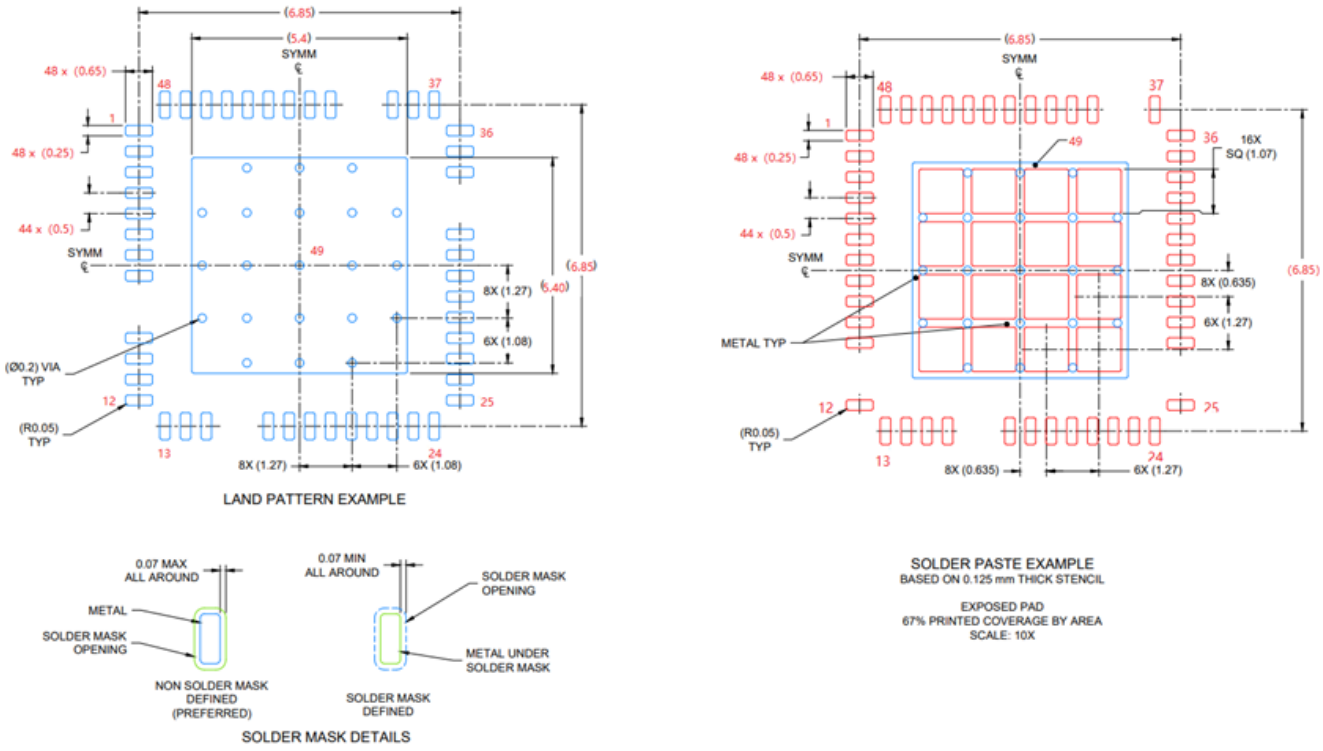
Figure 4. Package View

Table 50 provides detailed information about the dimensions.

Table 53. Dimensions

PARAMETER		SYMBOL	DIMENSIONS IN MILLIMETERS		
			MIN	NOM	MAX
Total Thickness		A	0.8	0.85	0.9
Stand Off		A1	0	0.02	0.05
Mold Thickness		A2	—	0.65	—
L/F Thickness		A3		0.203 REF	
Side Wettable Depth		A4	0.075	—	0.2
Lead Width		b	0.2	0.25	0.3
Body Size	X	D		7 BSC	
	Y	E		7 BSC	
Lead Pitch		e		0.5 BSC	
EP Size	X	D2	5.3	5.4	5.5
	Y	E2	5.3	5.4	5.5
Lead Length		L	0.3	0.4	0.5
		L1		0.4 REF	
Side Wettable Width		L1	0	—	0.075
Lead Tip to Exposed Pad Edge		K		0.4 REF	
Package Edge Tolerance		aaa		0.1	
Mold Flatness		ccc		0.1	
Coplanarity		eee		0.08	
Lead Offset		bbb		0.1	
Exposed Pad Offset		fff		0.1	

11. LAND PATTERN AND SOLDER PASTE EXAMPLE



Note: 请忽略上面两个图的管脚中间的空白，只是示意图，pin 没有连续放置，造成误解，敬请谅解，或许我们会尽快更新。

Figure 5. Land Pattern and Solder Paste Example

12. TAPE AND REEL INFORMATION

TBD

REVISION HISTORY

REVISION	DATE	DESCRIPTION
Rel 0.1	11 Feb 2023	0.1 DRAFT.
Rel 0.3	1 March 2023	Add TLE92108 info in English.
Rel 0.5	10 April 2023	Added more key features in
Rel 0.8	25 April 2023	Registers are added based on design New features are added in the doc
Rel 1.0	15 June 2023	Correct typ errors
Rel 1.1	17 July 2023	Added more info and translate to CN version.
Rel 1.1.1	18 July 2023	Remove DR7828Q related info as all functions are included in DR7808Q Correct format error on first page.
Rel 1.1.2	2 Auguest 2023	Updated Register Maps and EC table.