NSE34050Q-Q1

50mΩ, 40V, Automotive Quad Channel High-side Switch

Product Overview

NSE34050Q-Q1 is a quad channel 50mΩ high-side switch with protection and diagnostics for 12V automotive system applications. It's designed for driving all types automotive resistive, inductive or capacitive loads.

This device provides advanced protective functions in fault conditions, such as overvoltage clamp, current limitation, thermal shutdown and off-state diagnosis.

A FaultRST pin can be used to latch or retry the output in case of fault.

A sense enable pin allows lower power dissipation when it is disabled.

Key Features

- AEC-Q100 qualified for Grade 1:
  - Junction temperature(T_J) range from -40°C to 150°C
- Quad-Channel 50mΩ high-side switch
- Operating voltage range 4-28V with 40V load dump capability
- High-Accuracy Current Sense: ±25% Under 200- mA Load
- Protections
  - Current limit: 27A(NSE34050Q-Q1)/8A (NSE34051Q-Q1)
  - 48V overvoltage clamp for inductive loads protection
  - Thermal shutdown protection
  - Thermal swing protection when ΔT exceeds 60°C
  - Loss of ground and loss of Vcc protection
  - Undervoltage shutdown
  - Reverse battery protection with turning the power MOS on
- Full fault diagnostic:
  - Thermal shutdown diagnosis
  - Off-state open-load diagnosis
  - Output short to Vcc diagnosis
  - Current limitation or output short to ground diagnosis
- Low standby current: <500nA
- Enhanced low electromagnetic susceptibility

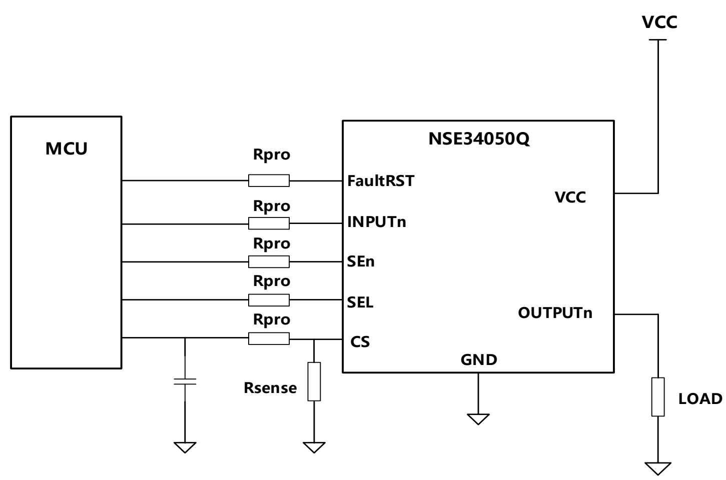
Applications

- All types automotive resistive, inductive or capacitive loads
- Driving high inrush current loads

Device Information

Part Number	*Package*	*Body Size*
NSE34050Q-Q1	PowerSSO-16	4.9mm x 3.9mm
NSE34051Q-Q1	PowerSSO-16	4.9mm x 3.9mm

Typical Application



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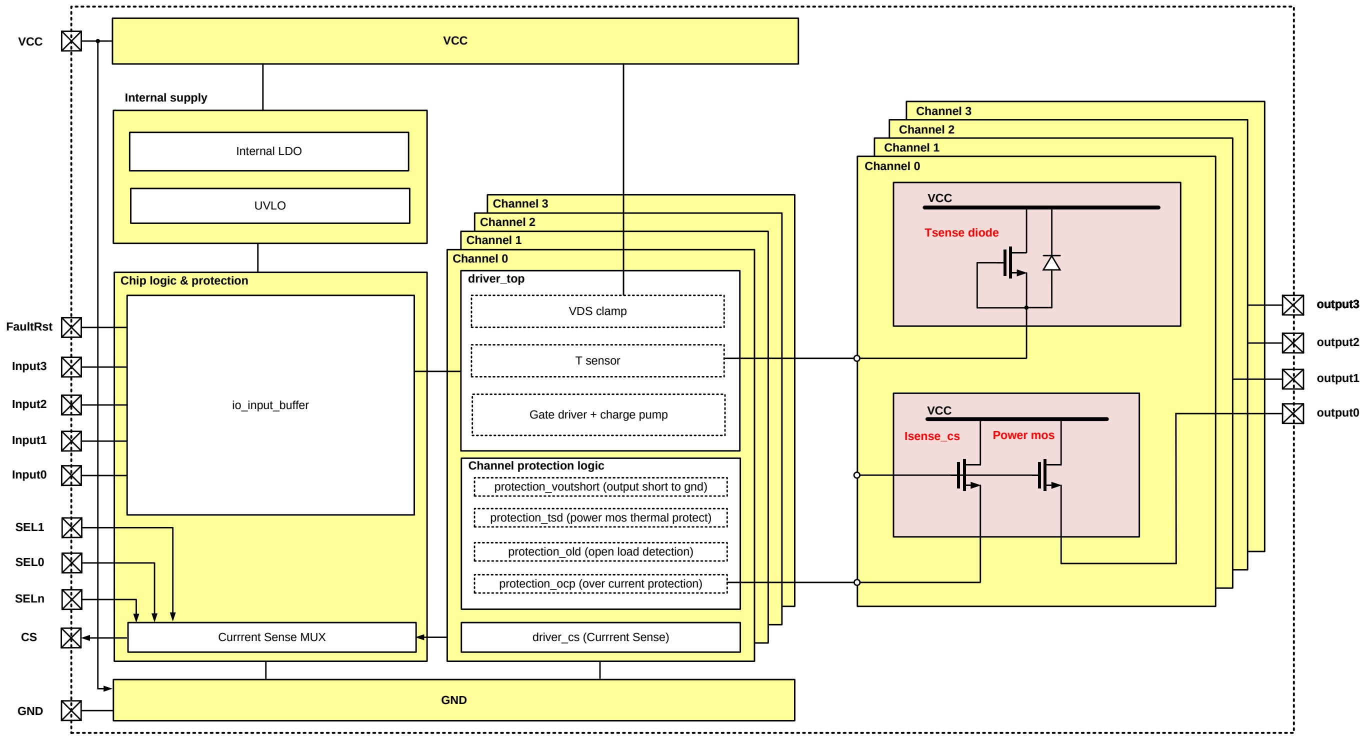
1. Block diagram



2. Pin Configuration and Functions

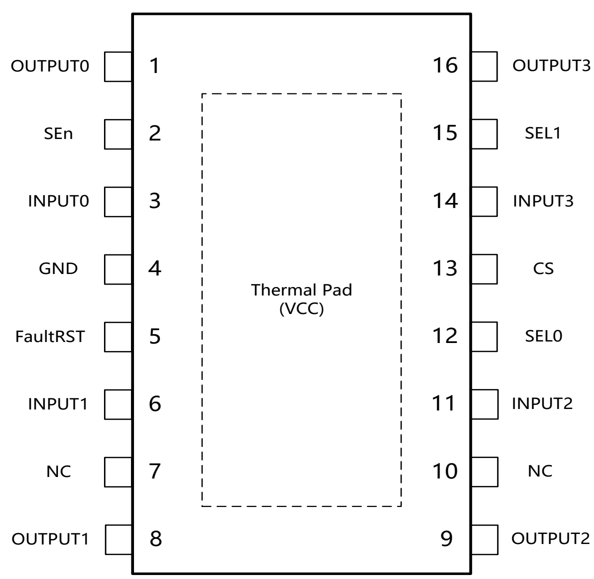


Figure 1 Pin Configuration

Table 1 PowerSSO-16 Pin Configuration and Description

PIN NO.	SYMBOL	FUNCTION
1, 8, 9, 16	$OUTPUT_{0,1,2,3}$	Power output.
2	SEn	Digital signal enables the CS diagnostic pin, active high.
3, 6, 11, 14	$INPUT_{0,1,2,3}$	Digital signal to control the channel n on/off, active high.
4	GND	Ground connection.
5	FaultRST	Digital signal to control the device auto-retry or latch-off in case of fault. The device works in auto-retry mode when it keeps low.
7, 10	N.C.	Not connect.
12, 15	$SEL_{0,1}$	Current sense channel select.
13	CS	Current sense output.

3. Recommended Connections for Unused Pins

Table 2 Recommended connections for unused pins

PIN NAME	CONNECTIONS FOR UNUSED PINS	IMPACT IF NOT USED
$OUTPUT_{0,1,2,3}$	Floating	No output.
SEn	Floating or ground through 15kΩ resister	Current sense is not available.
$INPUT_{0,1,2,3}$	Floating or ground through 15kΩ resister	All channel is off.
FaultRST	Floating or ground through 15kΩ resister	Default auto-retry mode.
$SEL_{0,1}$	Floating or ground through 15kΩ resister	Can not select current sense channel.
CS	To ground through 1kΩ resister, floating is not allowed	Current sense is not available.

4. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit
DC supply voltage	V_{cc}			40	V
Reverse DC supply voltage	$-V_{cc}$	-0.3			V
Maximum jump start voltage	V_{ccjs}			28	V
Reverse ground pin current	$-I_{GND}$	-200			mA

Parameters	Symbol	Min	Typ	Max	Unit
OUTPUT DC current	I_{out}			Internally limited	A
Reverse OUTPUT DC current	$-I_{out}$	Load limited			A
INPUT DC input current	I_{IN}	-1		10	mA
SEn DC input current	I_{SEn}				
SEL DC input current	I_{SEL}				
FaultRST DC input current	I_{FR}				
FaultRST DC input voltage	V_{FR}			7.5	V
CS pin DC output current	I_{snese}	-20		10	mA
Single pulse avalanche energy(L = 1mH, T_j = 150°C)	E_{AS}			24	mJ
Electrostatic discharge, Human-body model	HBM	-4000		4000	V
Electrostatic discharge, Charged-device model	CDM	-750		750	V
Junction Temperature	T_J	-40		150	°C
Storage Temperature	T_{stg}	-55		150	°C

5. Thermal Information

Parameters	Symbol	Value	Unit
IC Junction-to-ambient Thermal Resistance[1),2)]	θ_{JA}	25	°C/W
IC Junction-to-board Thermal Resistance[1),2)]	θ_{JB}	7.9	°C/W

Notes:

1). One channel ON.

2). Four layers 2s2p PCB JEDEC JESD 51-7

6. Specifications

6.1. Electrical Characteristics

(VCC = 7 V to 28 V, Tj =-40°C to 150°C, unless otherwise noted, All typical value refer to VCC = 13 V, Tj = 25°C, unless otherwise noted.)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Section						
Operating supply voltage	V_{cc}	4	13	28	V	
Undervoltage lockdown falling voltage	V_{UVLOF}		3.3		V	

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Undervoltage lockdown rising voltage	V_{UVLOR}		3.6		V	
Undervoltage lockdown hysteresis	V_{UVhys}		300		mV	
ON-state resistance	R_{ON}		50		mΩ	Iout = 2 A; Tj = 25°C
				100	mΩ	Iout = 2 A; Tj = 150°C
				75	mΩ	Iout = 2 A; Tj = 25°C; Vcc = 4V
Vcc-output clamp voltage	V_{CLAMP}	45	48	55	V	Is = 20mA; Tj =-40°C to 150°C
Supply current in standby mode	I_{SB}			0.5	µA	Vcc = 13 V; V_{IN} = V_{OUT} = V_{FR} = V_{SEn} = $V_{SEL0,1}$ = 0V; Tj = 25°C
				3	µA	Vcc = 13 V; V_{IN} = V_{OUT} = V_{FR} = V_{SEn} = $V_{SEL0,1}$ = 0V; Tj = 125°C
Supply current in onstate mode without Iout	$I_{S(ON)}$		10	16	mA	Vcc = 13 V; V_{OUT} = V_{FR} = V_{SEn} = $V_{SEL0,1}$ = 0V; $V_{IN0,1,2,3}$ = 5V; $I_{OUT0,1,2,3}$ = 0A
GND current in onstate mode with Iout	$I_{GND(ON)}$			20	mA	Vcc = 13 V; V_{OUT} = V_{FR} = $V_{SEL0,1}$ = 0V; $V_{IN0,1,2,3}$ = V_{SEn} = 5V; $I_{OUT0,1,2,3}$ = 1A
Bode diode forward voltage	V_{BD}			0.7	V	Iout =-2 A; Tj = 150°C
Input$_{0,1,2,3}$ section						
Low-level input voltage	V_{IL}			0.9	V	
Low-level input current	I_{IL}	1			µA	VIN = 0.9V
High-level input voltage	V_{IH}	2.1			V	
High-level input current	I_{IH}			15	µA	VIN = 2.1V
Input hysteresis voltage	$V_{I(hyst)}$	0.2			V	
Input clamp voltage	V_{ICL}	5.3		7.5	V	IIN = 1 mA
			-0.7			IIN = -1 mA
FaultRST section						
Low-level input voltage	V_{FRL}			0.9	V	
Low-level input current	I_{FRL}	1			µA	VIN = 0.9V
High-level input voltage	V_{FRH}	2.1			V	
High-level input current	I_{FRH}			15	µA	VIN = 2.1V

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Input hysteresis voltage	$V_{FR(hyst)}$	0.13			V	
Input clamp voltage	V_{FRCL}	5.3		7.5	V	IIN = 1 mA
			-0.7			IIN = -1 mA
$SEL_{0,1}$ section						
Low-level input voltage	V_{SELL}			0.9	V	
Low-level input current	I_{SELL}	1			µA	VIN = 0.9V
High-level input voltage	V_{SELH}	2.1			V	
High-level input current	I_{SELH}			15	µA	VIN = 2.1V
Input hysteresis voltage	$V_{SEL(hyst)}$	0.13			V	
Input clamp voltage	V_{SELCL}	5.3		7.5	V	IIN = 1 mA
			-0.7			IIN = -1 mA
SEn section						
Low-level input voltage	V_{SEnL}			0.9	V	
Low-level input current	I_{SEnL}	1			µA	VIN = 0.9V
High-level input voltage	V_{SEnH}	2.1			V	
High-level input current	I_{SEnH}			15	µA	VIN = 2.1V
Input hysteresis voltage	$V_{SEn(hyst)}$	0.13			V	
Input clamp voltage	V_{SEnCL}	5.3		7.5	V	IIN = 1 mA
			-0.7			IIN = -1 mA
Switching characteristics (VCC = 13V, Tj =-40°C to 150°C)						
Turn-on delay time	$t_{d(ON)}$	10	25	70	µs	RL = 6.5 Ω, VCC = 13 V, Tj = 25°C
Turn-off delay time	$t_{d(OFF)}$	10	25	70	µs	RL = 6.5 Ω, VCC = 13 V, Tj = 25°C
Turn-on slew rate	dv/dt_{on}	0.2	0.25	0.65	V/µs	RL = 6.5 Ω, VCC = 13 V, Tj = 25°C
Turn-off slew rate	dv/dt_{off}	0.2	0.35	0.65	V/µs	RL = 6.5 Ω, VCC = 13 V, Tj = 25°C
Switching energy losses at turn-on	W_{ON}	0.1	0.2	0.3	mJ	RL = 6.5 Ω, VCC = 13 V
Switching energy losses at turn-off	W_{OFF}	0.1	0.2	0.3	mJ	RL = 6.5 Ω, VCC = 13 V

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Pulse skew time (t_{PHL}- t_{PLH})	t_{SKEW}	-30	10	40	µs	RL = 6.5 Ω, VCC = 13 V
Protections						
DC short-circuit current	I_{limit}	21	27	38	A	VCC = 13 V, VIN = 5V
Deglitch time			1		µs	
Auto-retry times in case of fault after the Counter reset	$n_{RETRY(CR)}$	-	5	-		See Figure
Auto-retry times in case of fault after the first t_{RETRY} activation	$n_{RETRY(NT)}$	-	1	-		
Retry cycles allowed before channel latch off	$n_{RETRY(CYC)}$	-	2	-		
Auto-retry time after fault condition	t_{RETRY}	40	70	100	ms	
Counter reset delay time after fault condition	$t_{DELAY(CR)}$	40	70	100	ms	
Shutdown temperature	T_{TSD}	150	175	200	°C	
Reset temperature	T_R	T_{RS} + 1	T_{RS} + 7		°C	
Thermal reset of diagnostic indication	T_{RS}	135			°C	V_{FR} = 0V, V_{SEn} = 5V
Thermal hysteresis (TTSD- TR)	T_{HYST}		7		°C	
Dynamic temperature	ΔTj		60		K	Tj =-40°C, VCC = 13V
Dynamic temperature hysteresis	ΔTj(HYS)		20		K	
Fault reset time for output unlatch	t_{LATCH_RST}	3	14	20	µs	V_{FR} = 5V to 0V, V_{SEn} = 5V
Turn off output voltage clamp	V_{DEMAG}	V_{CC}-45	V_{CC}-48	V_{CC}-55	V	Tj =-40°C to 150°C
CS pin to ground clamp voltage	V_{CSG_CL}		7		V	I_{SENSE} = 1mA, VCC = 13V
Current Sense						
K_0	I_{OUT}/I_{SEN}	-30%	1200	30%		I_{OUT} = 0.01A to 0.05A, V_{sense} = 0.5V
K_1	I_{OUT}/I_{SEN}	-25%	1200	25%		I_{OUT} = 0.2A, V_{sense} = 0.5V
K_2	I_{OUT}/I_{SEN}	-20%	1200	20%		I_{OUT} = 0.4A, V_{sense} = 4V
K_3	I_{OUT}/I_{SEN}	-15%	1200	15%		I_{OUT} = 1.5A, V_{sense} = 4V
K_4	I_{OUT}/I_{SEN}	-10%	1200	10%		I_{OUT} = 4.5A, V_{sense} = 4V
				0.5		V_{SEn} = 0V

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
CS pin leakage current	I_{SENSE0}	-0.5		0.5	µA	V_{SEn} = 0V,-1V < V_{SENSE} < 5V
				10		V_{SEn} = 5V, I_{OUTx} = 0A, $V_{INPUT0,1,2,3}$ = 5V, channel diagnostic selected
				10		V_{SEn} = 5V, I_{OUTx} = 0A, $V_{INPUT0,1,2,3}$ = 0V, channel diagnostic selected
Output voltage for CS shutdown	V_{OUT_MSD}		4.6		V	V_{SEn} = 5V, R_{SENSE} = 1.2kΩ, I_{OUT} = 4.5A
CS saturation voltage	V_{SENSE_SAT}		4.6		V	VCC = 7V, V_{SEn} = 5V, R_{SENSE} = 2.7kΩ, I_{OUT} = 4.5A
CS saturation current	I_{SENSE_SAT}	4			mA	VCC = 7V, V_{SEn} = 5V, V_{SENSE} = 4V, V_{INPUT} = 5V, Tj = 150°C
Output saturation current	I_{OUT_SAT}	4.8			A	VCC = 7V, V_{SEn} = 5V, V_{SENSE} = 4V, V_{INPUT} = 5V, Tj = 150°C
Off-state diagnostic						
Off-state open-load voltage detection threshold	V_{OL}	2	3	4	V	V_{SEn} = 5V, V_{INPUT} = 0V
Off-state output sink current	$I_{L(off)}$	-25		-5	µA	V_{INPUT} = 0V, V_{OUT} = V_{OL}
Off-state diagnostic delay time from falling edge of INPUT	t_{DSTKON}	100	350	700	µs	V_{SEn} = 5V, V_{INPUT} = 5V to 0V
Setting time for valid Off-state open-load diagnostic indication from rising edge of SEn	$t_{D\_OL\_V}$			60	µs	V_{SEn} = 0V to 5V
Off-state diagnostic delay time from rising edge of V_{OUT}	t_{D_VOL}		5	30	µs	V_{SEn} = 5V, V_{INPUT} = 0V, V_{OUT} = 0V to 4V
Fault diagnostic						
CS pin output voltage in fault condition	V_{SENSEH}	5		7.4	V	
CS pin output current in fault condition	I_{SENSEH}	5	7	15	mA	
Current sense timings						
CS setting time from rising edge of SEn	$t_{DSENSE1H}$			50	µs	V_{SEn} = 0V to 5V, V_{INPUT} = 5V, R_{SENSE} = 1kΩ, R_L = 6.5Ω
CS disable time delay from falling edge of SEn	$t_{DSENSE1L}$			2	µs	V_{SEn} = 5V to 0V, R_{SENSE} = 1kΩ, R_L = 6.5Ω

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
CS setting time from rising edge of INPUT	$t_{DSENSE2H}$		60	100	µs	V_{SEn} = 5V, V_{INPUT} = 0V to 5V, R_{SENSE} = 1kΩ, R_L = 6.5Ω
CS setting time from rising edge of I_{OUT} (dynamic response to a step change of I_{OUT})	$\Delta t_{DSENSE2H}$			100	µs	V_{SEn} = 5V, V_{INPUT} = 5V, R_{SENSE} = 1kΩ, R_L = 6.5Ω
CS turn off delay time from falling edge of INPUT	$t_{DSENSE2L}$		50	250	µs	V_{SEn} = 5V, V_{INPUT} = 5V to 0V, R_{SENSE} = 1kΩ, R_L = 6.5Ω

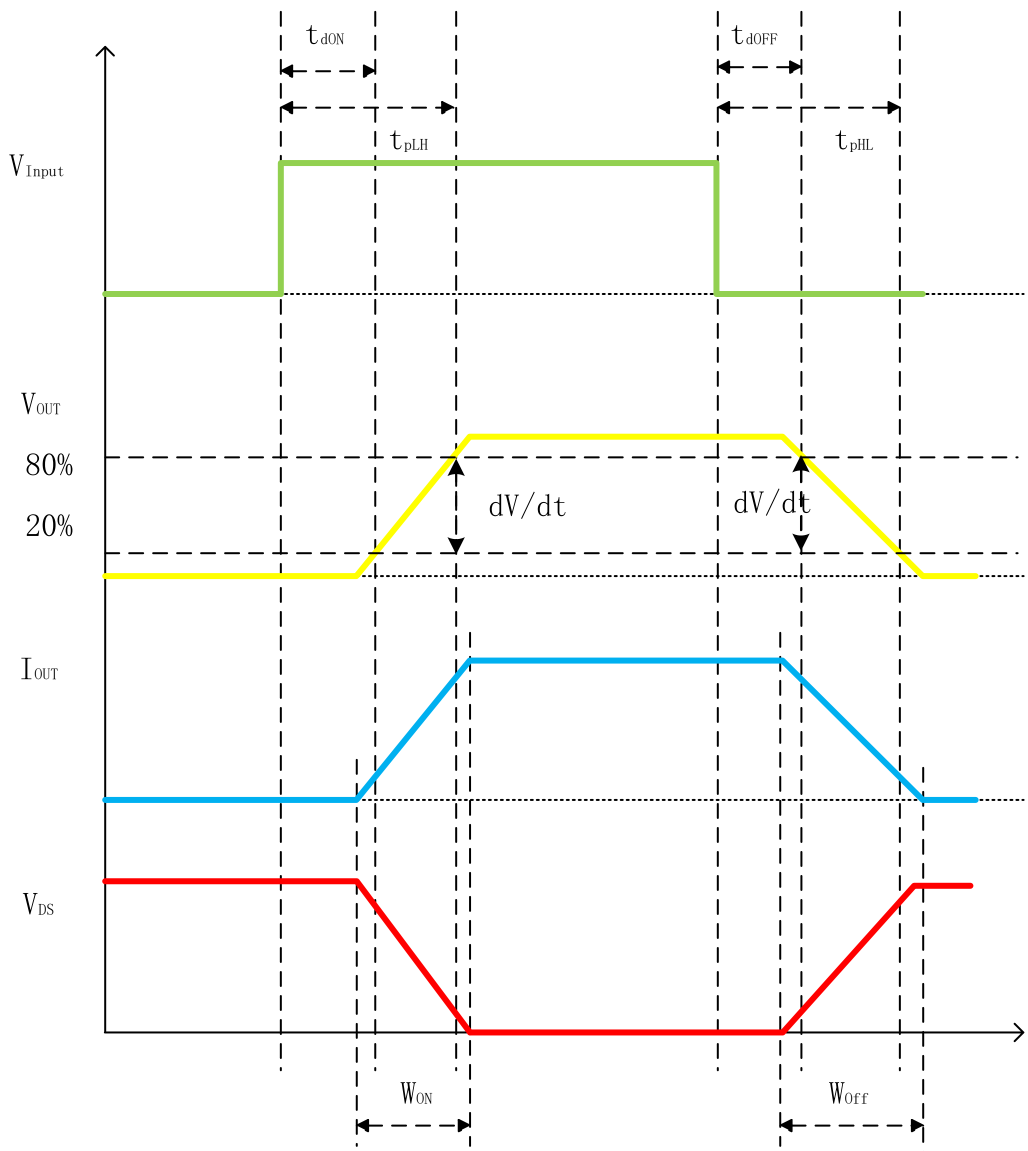


Figure 2 Switching times and switching loss

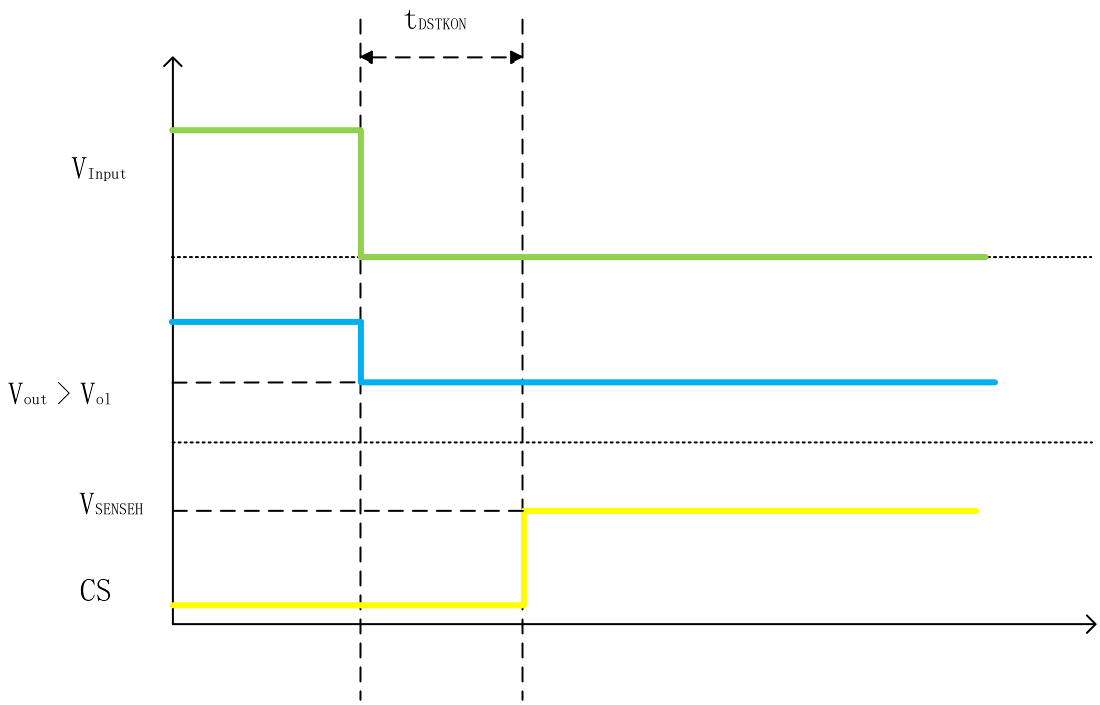


Figure 3 Off-state diagnostic delay time from falling edge of INPUT

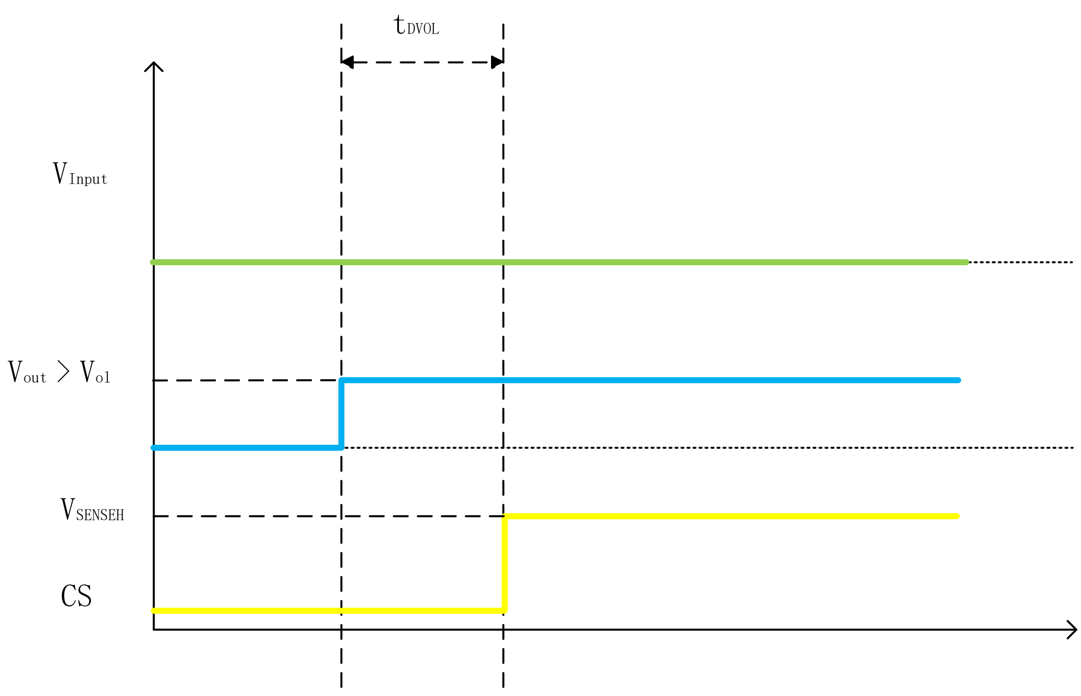


Figure 4 Off-state diagnostic delay time from rising edge of VOUT

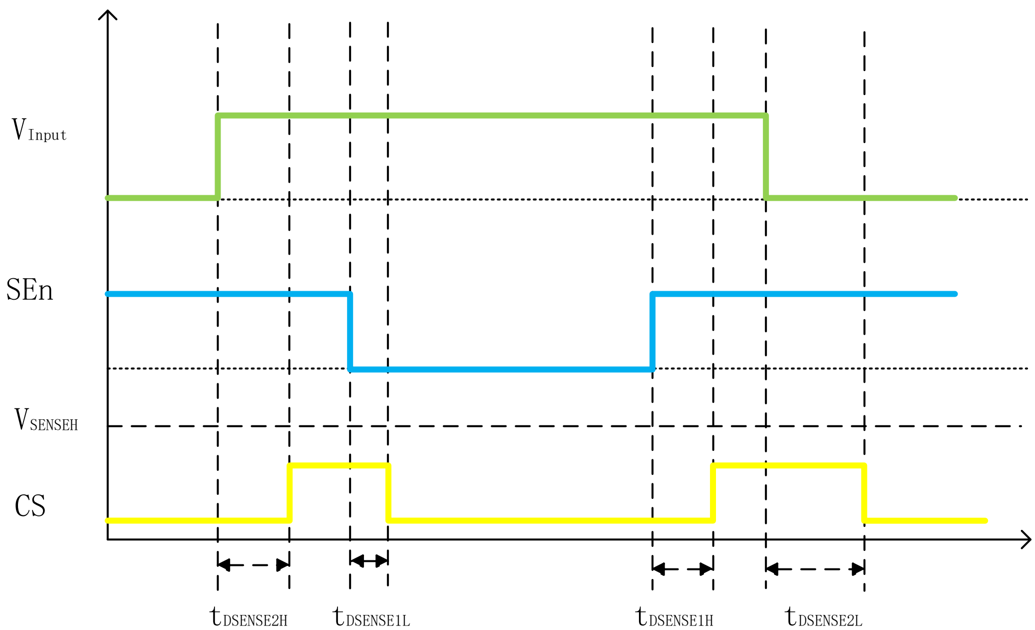


Figure 5 Current sense timing

6.2. Typical Performance Characteristics

6.2.1. True table

Mode	*Conditions*	*IN_X*	*FR*	*SEn*	*SEL_X*	*OUT_X*	*CS*	*Comments*
Standby	All logic inputs low	L	L	L	L	L	Hi-Z	
Normal	Nominal load connected, Tj < 150°C	L	X	Refer to CS address		L	Refer to CS address	
		H	L			H	Refer to CS address	Outputs for auto-retry
		H	H			H	Refer to CS address	Outputs for latch-off
Overload	Overload or short to GND, Tj > 175 °C or ΔTj > 60k	L	X	Refer to CS address		L	Refer to CS address	
		H	L			H	Refer to CS address	
		H	H			L	Refer to CS address	
Under voltage	VCC < UVLO (falling)	X	X	X	X	L	Hi-Z	
Off-state diagnostics	Short to VCC	L	X	Refer to CS address		H	Refer to CS address	

Mode	*Conditions*	*IN_X*	*FR*	*SEn*	*SEL_X*	*OUT_X*	*CS*	*Comments*
	Open-load	L	X			H	Refer to CS address	External pull-up
Negative output voltage	Inductive load turn off	L	X	Refer to CS address		< 0V	Refer to CS address	

6.2.2. Current sense MUX address

SEn	*SEL0*	*SEL1*	*MUX channel*	*Normal mode*	*Overload*	*Off-state diag*	*Negative output*
L	X	X		Hi-Z			
H	L	L	Channel 0	I_{SENSE} = 1/K * I_{OUT0}	V_{SENSE} = V_{SENSEH}	V_{SENSE} = V_{SENSEH}	Hi-Z
H	L	H	Channel 1	I_{SENSE} = 1/K * I_{OUT1}	V_{SENSE} = V_{SENSEH}	V_{SENSE} = V_{SENSEH}	Hi-Z
H	H	L	Channel 2	I_{SENSE} = 1/K * I_{OUT2}	V_{SENSE} = V_{SENSEH}	V_{SENSE} = V_{SENSEH}	Hi-Z
H	H	H	Channel 3	I_{SENSE} = 1/K * I_{OUT3}	V_{SENSE} = V_{SENSEH}	V_{SENSE} = V_{SENSEH}	Hi-Z

7. Protections

7.1. Current limitation

NSE34050Q-Q1 has current limitation to protect the silicon and bonding wire in case of overload or short circuit to ground. In order to allow a higher load inrush at low ambient temperature, Overload threshold is related with VDS and temperature.

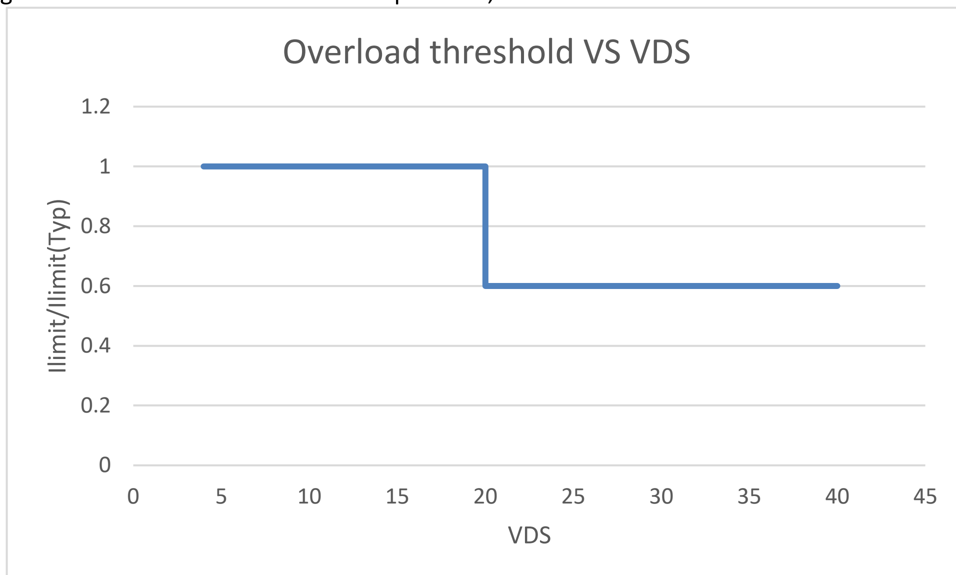


Figure 6 Overload current threshold VS VDS

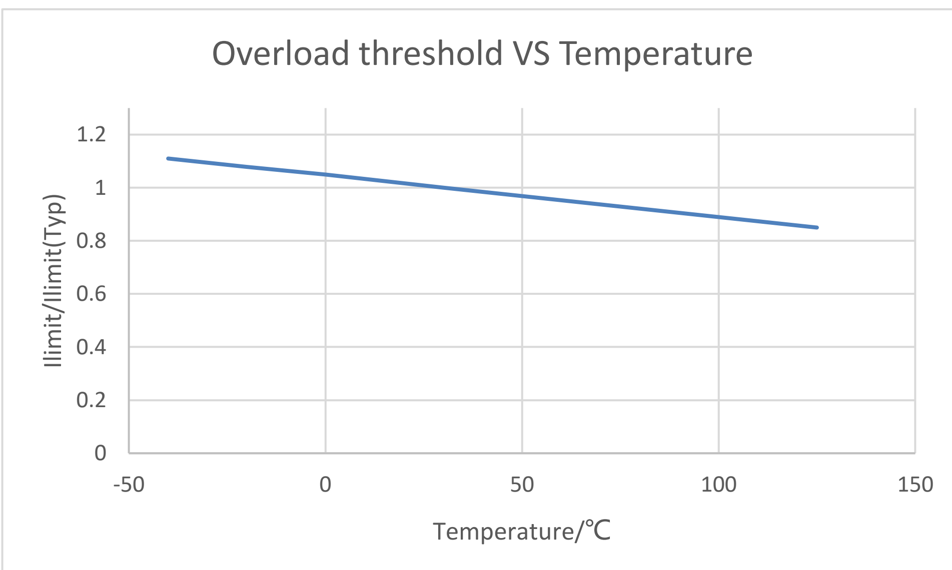


Figure 7 Overload current threshold VS temperature

7.1.1. Retry strategy

While the FaultRST pin is set to low, NSE34050 works in auto-retry mode. Then the channel can be allowed to restart only if all retry conditions have been fulfilled in case of fault condition.

In the fault condition, the channel will switched on for $n_{RETRY(CR)}$ times then switch off, after a time t_{RETRY}, the channel will switch on for $n_{RETRY(CYC)}$ retry cycles then latch off. It is necessary to set the input pin to low for a time longer than $t_{DELAY(CR)}$ to reset the internal counter to unlatch the channel. The auto-retry timing is shown in Figure 7 and the latch-up timing is shown in Figure 8.

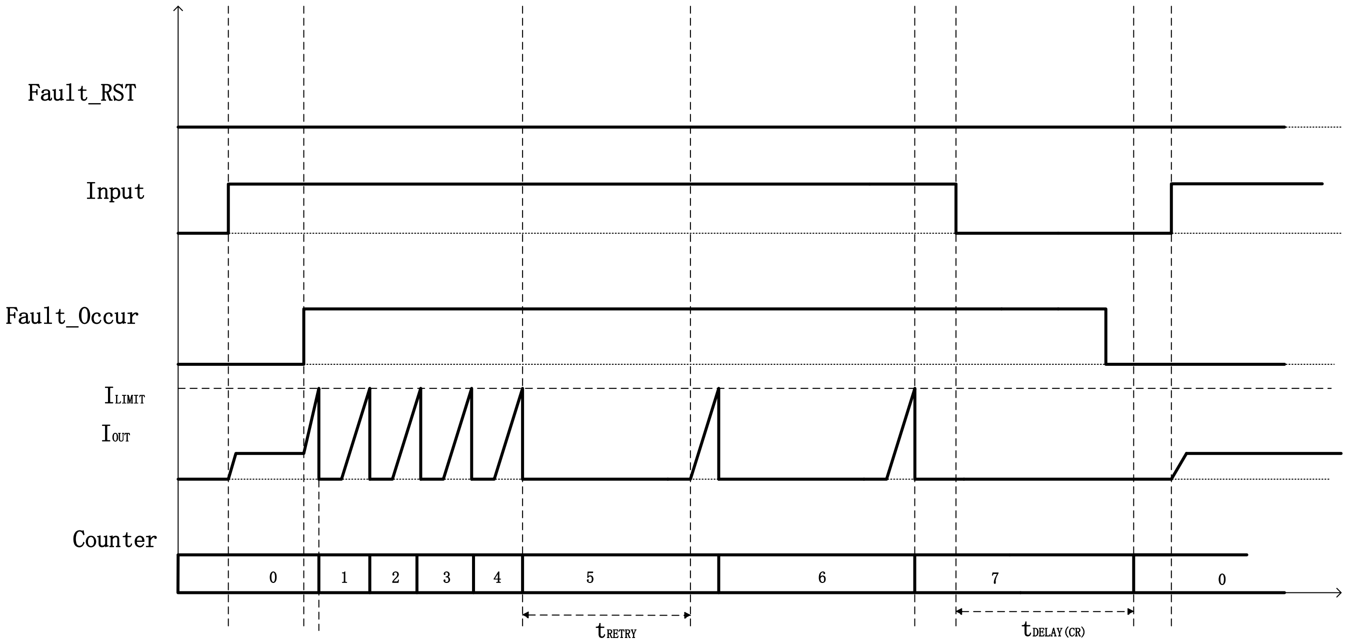
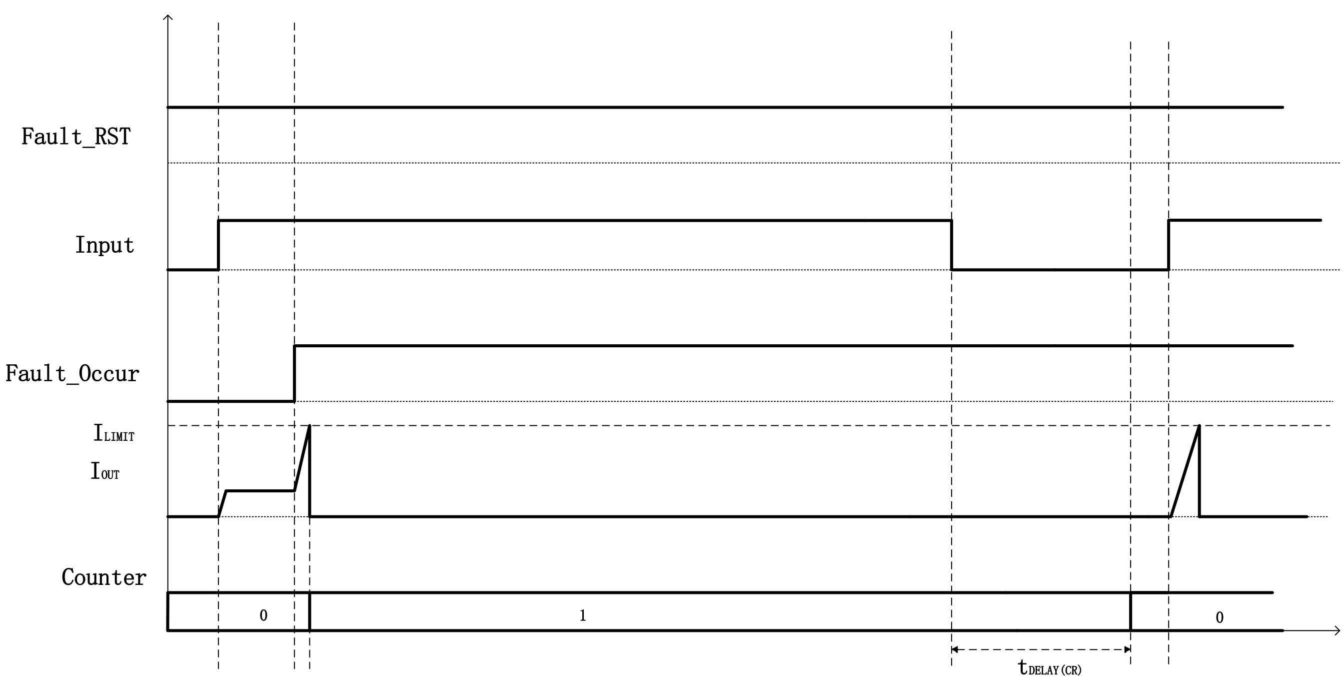


Figure 8 Auto-retry timing



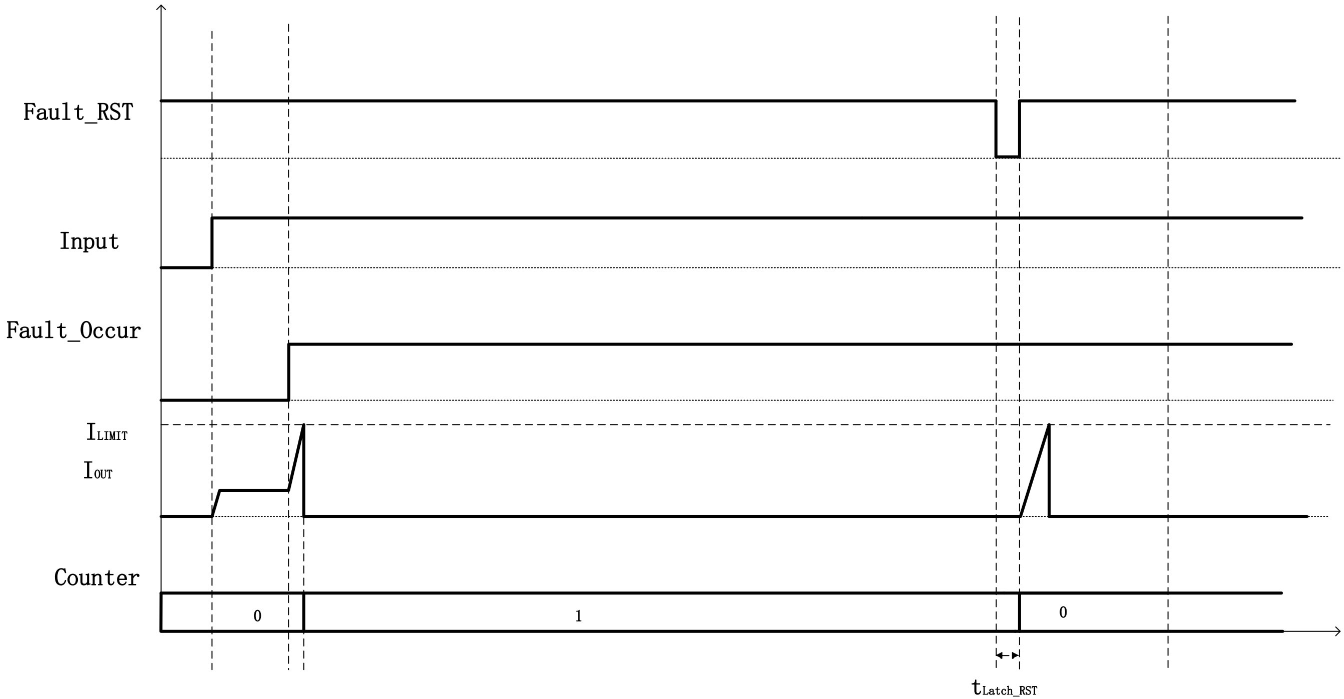


Figure 9 Latch-up timing

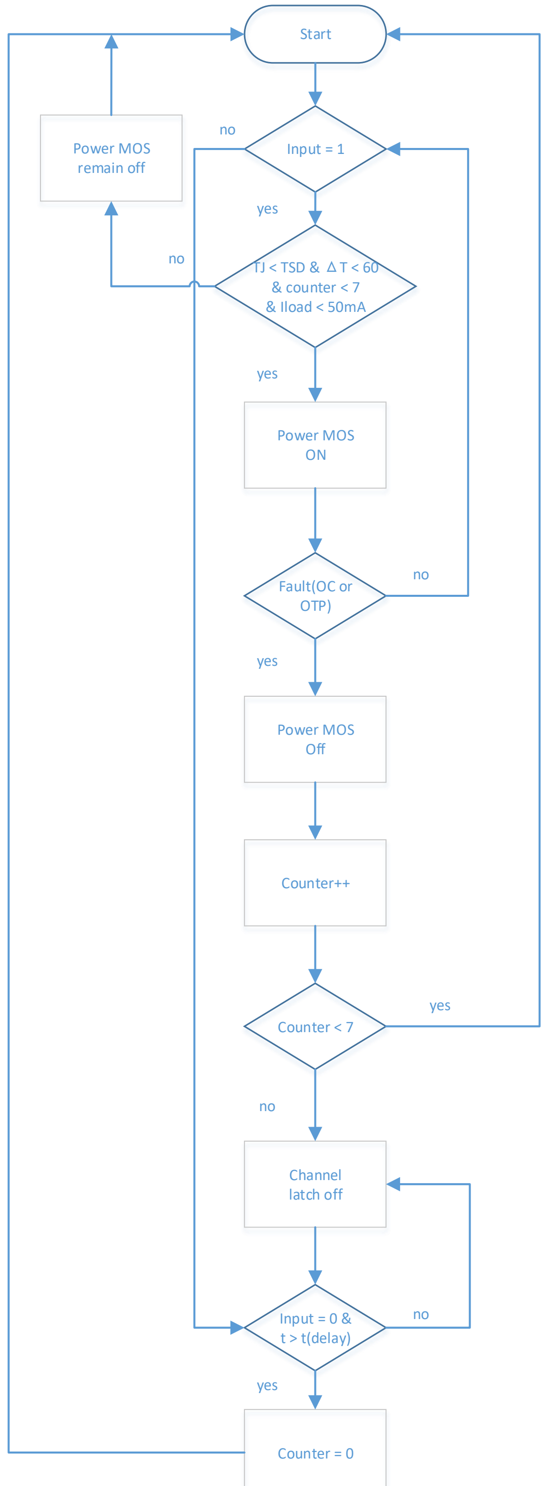


Figure 10 Retry strategy

7.2. Thermal shutdown and thermal swing

This device has both absolute and dynamic temperature protection. There are two thermal sensors on the controller and the MOSFET, the one on the MOSFET is the hottest and the one on the controller is the coldest. The absolute temperature protection is to shutdown the MOSFET when the hottest junction temperature exceeds the T_{TSD}, and the dynamic temperature protection is also to shutdown the MOSFET when the temperature difference between the hottest and the coldest exceeds ΔTj.

7.3. Inductive load voltage clamp

In the case device turns off when driving inductive load, the voltage between VCC and output will exceed VCC. VDS should be clamped to limit the voltage to protect the power MOSFET from breakdown. The clamp voltage is lower than BVDSS of the MOSFET, the energy of inductor is dissipated without damaging the device.

7.4. Reverse polarity protection

In reverse polarity condition, the device will switch on the power MOSFET, so that to reduce the power dissipation on the power MOSFET, which is limited by the load. If power MOSFET is off, reverse current will pass through body diode and cause more power dissipation which may damage the device. What's more, the device integrate a diode in the GND, so that it is not necessary to place a diode outside the GND pin to avoid the reverse current.

7.5. Loss of battery and loss of ground protection

When the load is inductive, then battery is loss of connection, it is recommended to place an external diode to handle the energy of inductor when loss of battery.
In case of loss ground, the power MOSFET will be ensured to switch off to avoid MOSFET on by mistake.

8. Application information

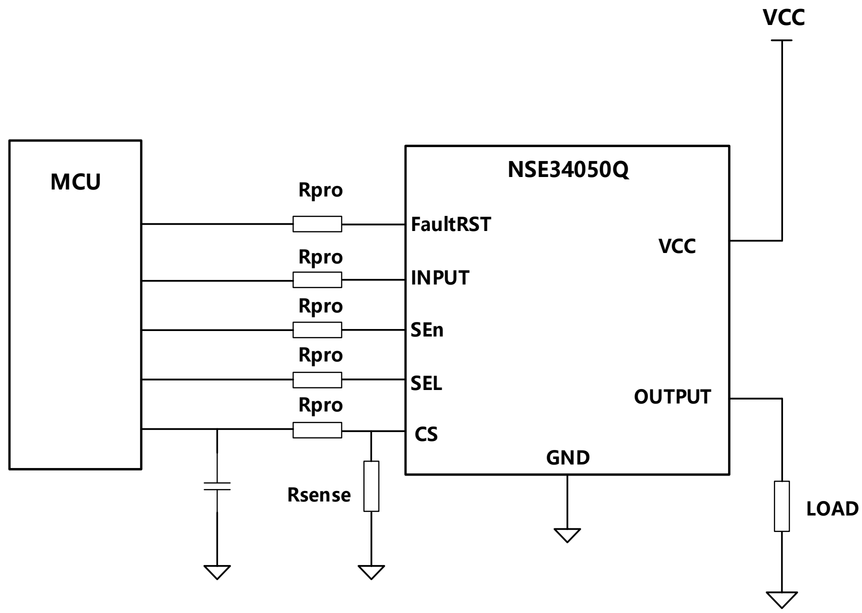


Figure 11 Typical application

9. Electrical characteristics curves

at VCC = 13 V (unless otherwise specified)

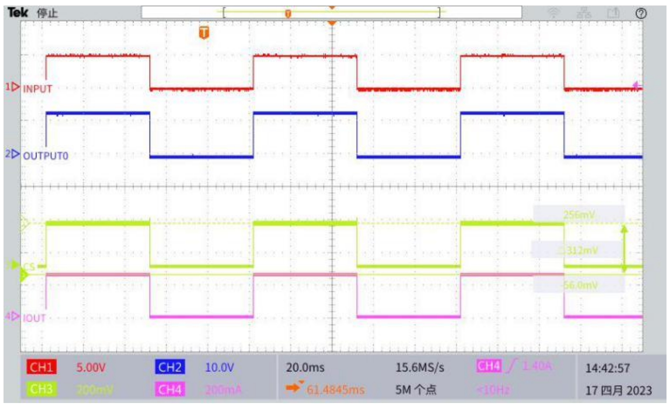


Figure9.1 Turn on/off

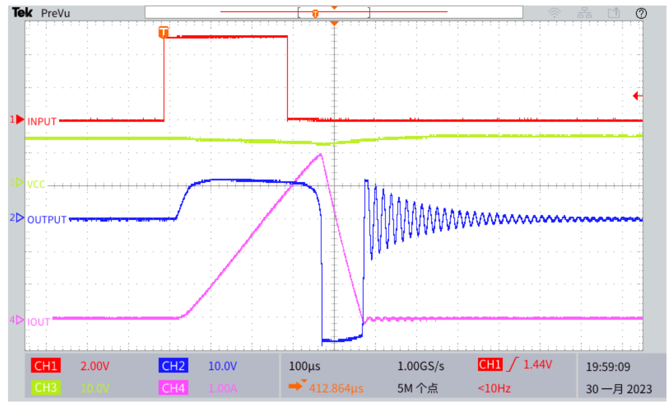


Figure9.2 VDS clamp

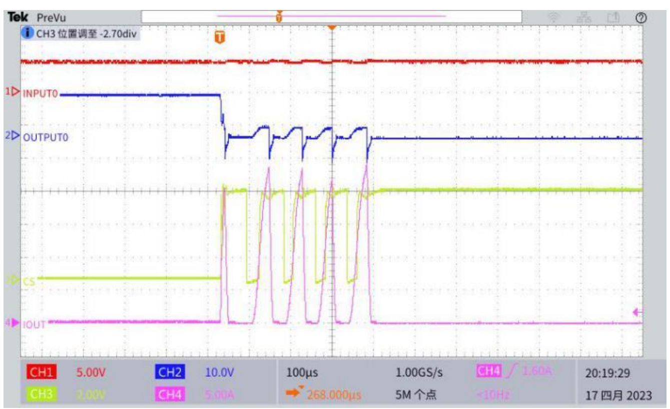


Figure9.3 Over current protection in retry mode

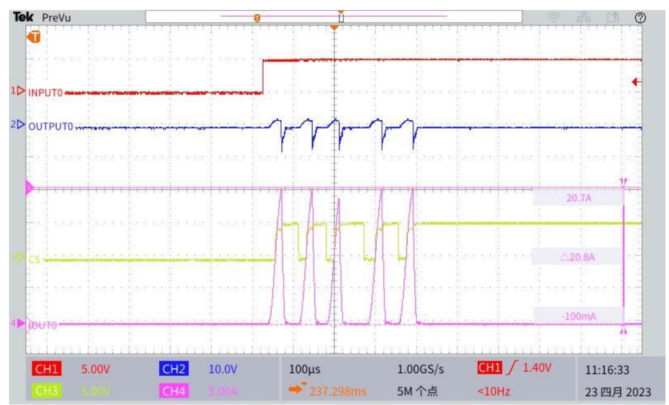


Figure9.4 Over current protection in retry mode @85℃

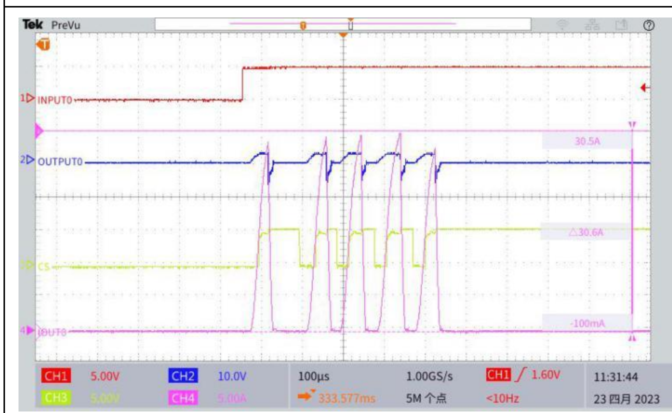


Figure9.5 Over current protection in retry mode @-40℃

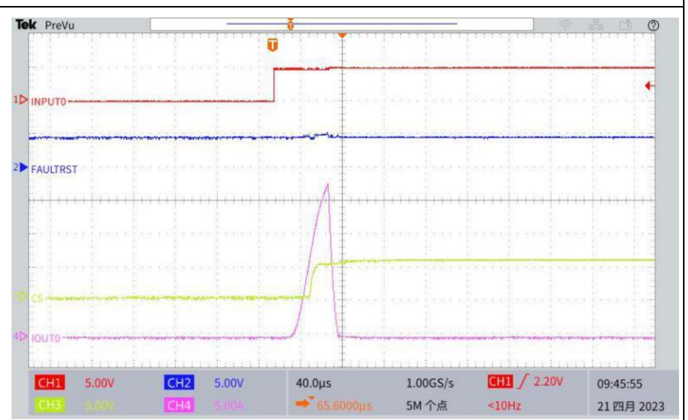


Figure9.6 Over current protection in latch mode

10. Immunity against transient electrical disturbances

11. Package and PCB thermal data

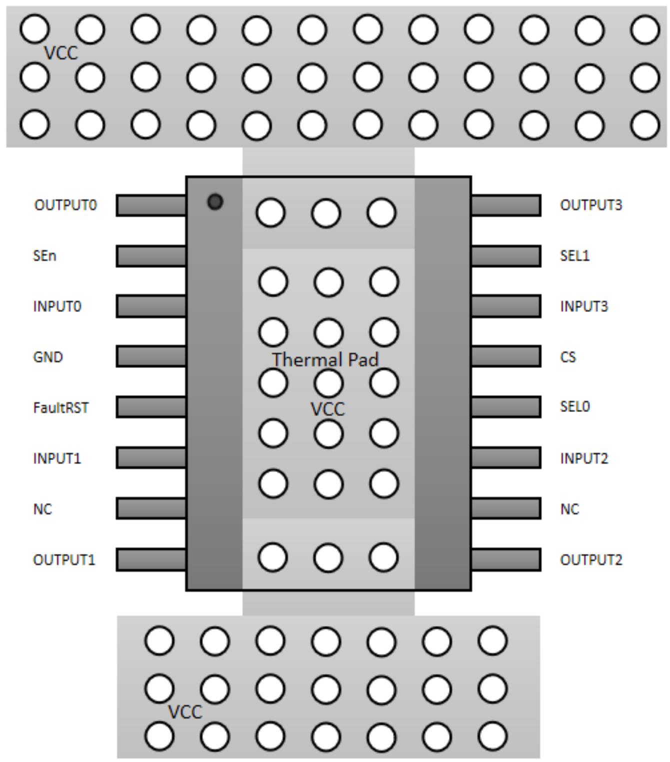
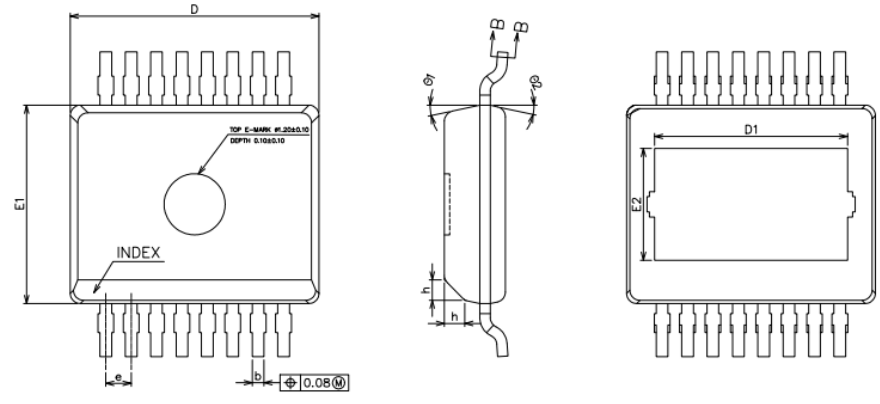


Figure 12 Layout example

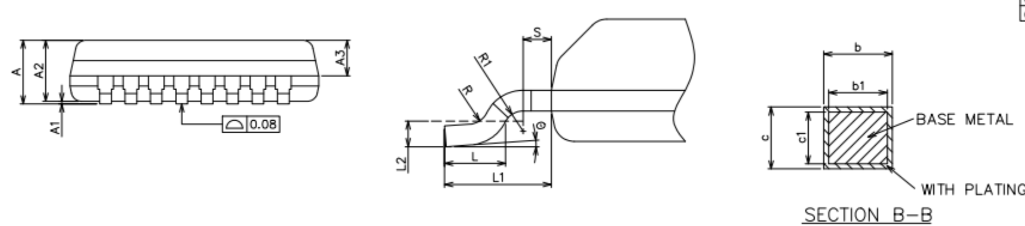
12. Package Information

12.1. PowerSSO-16



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL		MIN	NOM	MAX
A		–	–	1.40
A1		0.00	0.05	0.10
A2		1.10	1.20	1.30
A3		0.60	0.70	0.80
b	NiPdAu	0.20	–	0.28
	Pure Sn	0.21		0.30
b1		0.20	0.23	0.26
c	NiPdAu	0.19	–	0.25
	Pure Sn	0.20	–	0.28
c1		0.19	0.20	0.23
D		4.80	4.90	5.00
D1		3.60	3.80	4.00
E		5.80	6.00	6.20
E1		3.80	3.90	4.00
E2		2.00	2.20	2.40
e		0.40	0.50	0.60
h		0.30	0.40	0.50
L		0.40	0.60	0.85
L1		1.05REF		
L2		0.25BSC		
R		0.07	–	–
R1		0.07	–	–
S		0.20	–	–
θ		0°	–	8°
θ1		10°	12°	14°
θ2		10°	12°	14°
θ3		10°	12°	14°
θ4		10°	12°	14°



13. Revision history

Revision	Description	Date
0V1	Initial version	2022/03
0V2	Some updates	2022/08
0V3	Package information	2023/01
0V4	Add some curves	2023/05
0V5	Modification on 1st page	2023/06